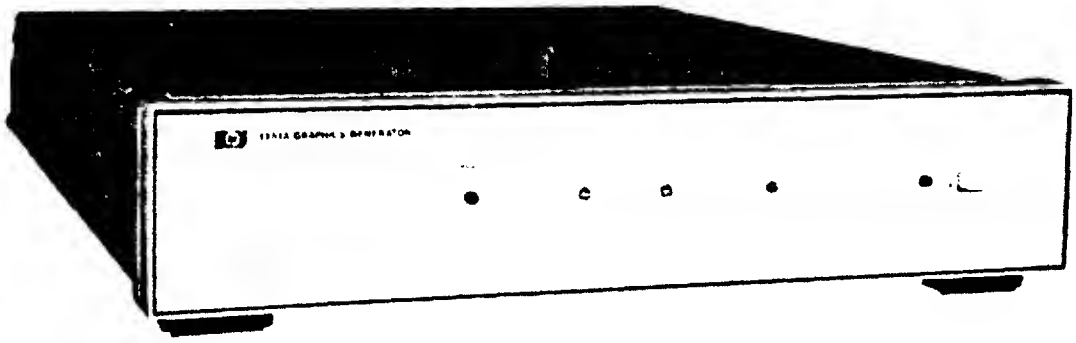
OPERATING AND SERVICE MANUAL

1351A

52105A RS-232C (1351A OPTION 001) INTERFACE



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SAFETY

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual, must be heeded. Refer to Section I and the Safety Summary for general safety considerations applicable to this product.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

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This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. However, warranty service for products installed by HP and certain other products designated by HP will be performed at Buyer's facility at no charge within the HP service travel area. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

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SCW & A 9/78

OPERATING AND SERVICE MANUAL

52105A RS-232C (1351A OPTION 001) INTERFACE FOR THE MODEL 1351A

CONFIGURATION CODES

This manual applies directly to boards with configuration code **2138.**

Manual Part Number 52105-90902
Microfiche Part Number 52105-90802

PRINTED: NOVEMBER 1981

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

This manual provides the interface information necessary to operate an HP Model 1351A/Option 001 (RS-232C) Graphics Translator in a system configuration. The 1351A/Option 001 contains an HP Model 52105A RS-232C I/O board. The characteristics of the 1351A/Option 001 are listed in table 1-1. For more detailed operating and service information, refer to the 1351A Operating and Programming Manual, and to the 1351A Operating and Service Manual.

1-2. CHARACTERISTICS.

The 1351A/Option 001 52105A (RS-232C) characteristics are described in table 1-1.

Table 1-1. 1351A/Option 001 and 52105A Characteristics

CONNECTIONS

RS-232: 25 pin male connector.

AUXILLIARY: 25 pin female connector to interface to a Hewlett-Packard Model 1338A Tri-Color Display

DISPLAY: Four BNC female connectors to control the unblanking of up to four (4) displays.

RS-232 CONFIGURATION

The 1351A/001 interface is a Modem as described by the RS-232C specification.

SIGNAL LEVELS: Low = <-3 volts; High = >+3 volts.

DATA INPUT: Mark = 1 = Low; Space = 0 = High.

DATA FORMAT

Data Length: 7 or 8 bits, switch selectable.

Stop Bits: 1 or 2 bits, switch selectable.

Parity: switch selectable to either transmit with or without parity. Switch selectable to either transmit with either even or odd parity.

BAUD RATE

Sixteen switch-selectable baud rates: 50, 75, 110, 134.5, 150, 300, 600, 900, 1200, 1800, 2400, 3600, 4800, 7200, 9600, and 57600.

EXTERNAL CLOCK

The 52105A can provide a gated clock to control the flow of data from a controller into the 1351A/Option 001.

CLOCK OUTPUT: RS-232C level on pin 15 of the interface connector. Gated with H = Ready to stop clocking when the 1351A is busy. Clock stops at its high level. Clock rate is 16 X baud rate.

TTL level output on pin 16 of the interface connector. Clock rate is 8 X baud rate. This can be changed to 16 X baud rate via P.C. board jumpers. Clock stops at its low level.

CLOCK INPUT: The 52105A can accept an external clock from the controller supplying data to the 1351A/Option 001 to allow the data source to control the baud rate.

Level: RS-232C levels.

Clock Rate: Baud rate X 16.

CONTROL FLAGS

CLEAR TO SEND: an output of the 1351A/Option 001 on pin 5 of the interface connector. Used to synchronize the flow of data in to the 1351A in conjunction the Request To Send flag.

Levels: RS-232C levels; Low = 1351A is busy and can not accept data; High = 1351A is available to receive data.

REQUEST TO SEND: an input to the 1351A/Option 001 on pin 4 of the interface connector. Used to conjunction with the Clear To Send flag to synchronize the flow of data into the 1351A.

Levels: RS-232C levels; Low = Interface is reset; High = 1351A is enabled for data.

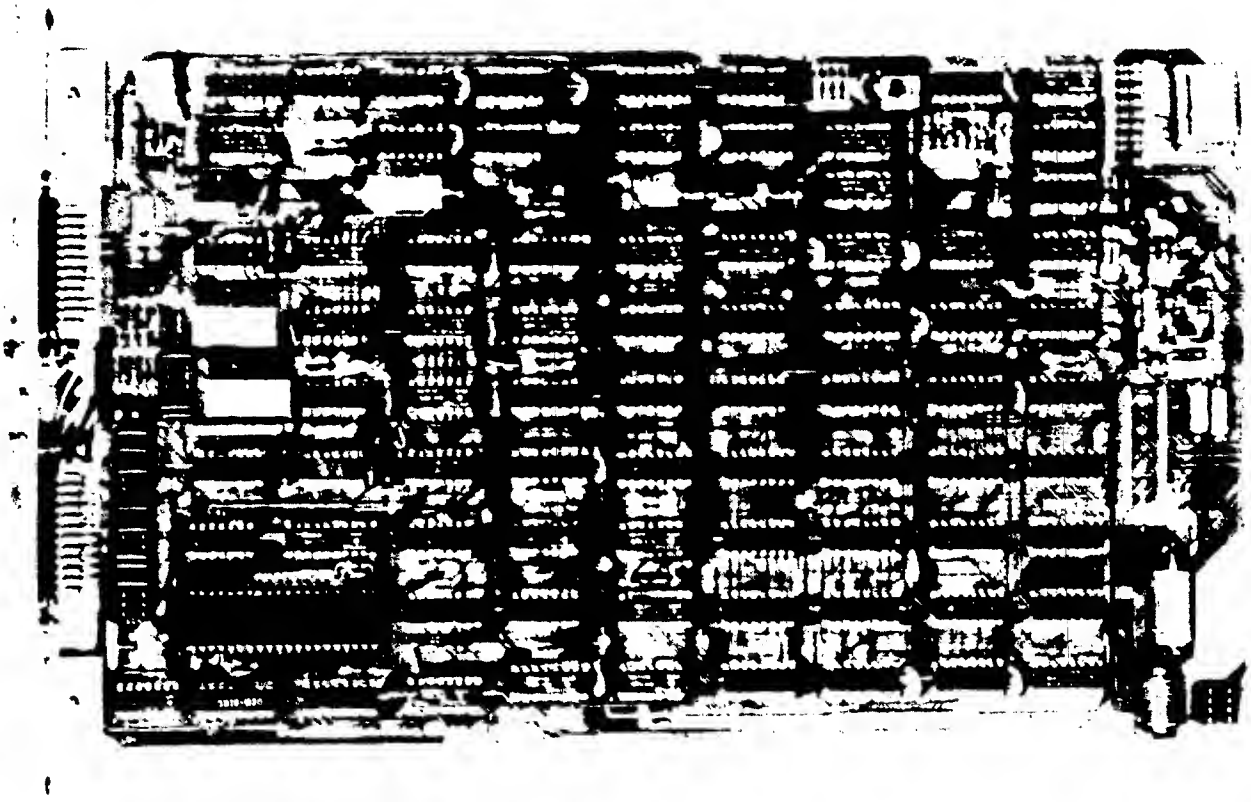


Figure 1-1. Model 52105A RS-232C Interface

1-3. DESCRIPTION.

The 1351A Option 001 is supplied with the 52105A RS-232C interface installed (see figure 1-1). This interface is very flexible and many configurations may be supported. It is shipped from the factory in the RS-232C modem configuration. However, it differs from the normal modem configuration in that a male connector is provided (see figure 1-2). This is done to prevent the RS-232C interface bus from being connected to the 1351A auxiliary output. Table 1-2 describes the input and output signals on the RS-232C interface connector of the 52105A interface module.

1-4. TERMINALS AND NULL MODEMS.

It is impossible to directly connect two RS-232C compatible terminals together. For instance, if pin 2 is connected between the terminals, they would both be trying to transmit data out on the same line. A more reasonable connection would be to cross pin 2 on terminal A to pin 3 on terminal B and cross pin 2 on terminal B to pin 3 on terminal A. This, then, is the purpose of the infamous "Null Modem". The null modem can take the form of a cable like the one provided with the RS-232C interface for the 1351A, or a circuit card with connection pins and/or switches. The function of a

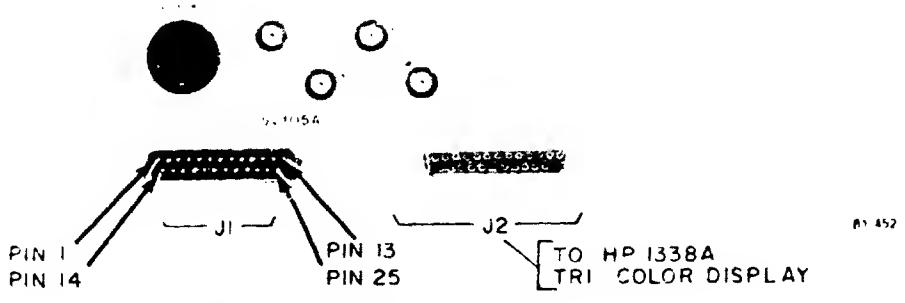


Figure 1-2. Model 52105A I/O Connectors

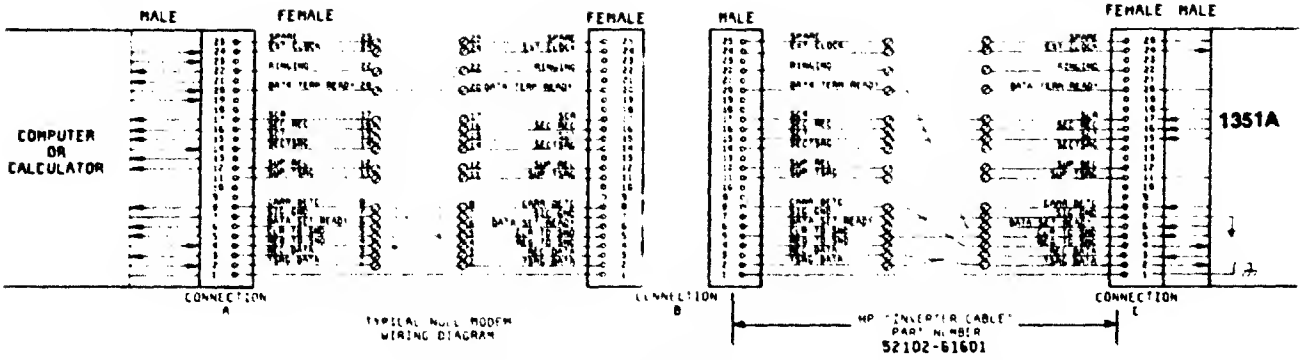


Figure 1-3. Wiring Diagrams for Systems Which Utilize Null Modes

Table 1-2. Interface Functions Supported by 1351A/ Option 001 and 52105A

Pin no.	Direction	Name and/or Function
1		Protective ground, shield.
2	into 1351A	Transmitted data, serial ASCII data in.
3	out of 1351A	Received data, serial ASCII data out.
4	in	Request To Send, resets the 1351A interface.
5	out	Clear To Send, tells the computer/ calculator that a transmission can start or must stop.
6	out	Data Set Ready, power is "on" in the 1351A
7	-	Signal ground, common return.
8	out	Carrier detect, tied to Clear To Send.
15	out	Transmission clock, clock signal is RS-232 voltage level compatible and is suitable for operating the transmit portion of the RS-232 interface at the remote end. Clock rate is baud rate X 16.
16	out	Transmission clock, clock is TTL signal level compatible and is suitable for operating an RS-232 interface card on the HP System 1000 (with modified 12531C card). Clock rate is baud rate X 8, can be changed to X 16 with jumper.
17	out	Transmission clock, clock signal is RS-232 voltage level compatible and is suitable for operating the receiver portion of the RS-232 interface at the remote end. Clock rate is baud rate X 16.
20		Undefined, user option.
24	in	Receive clock, clock signal is RS-232 voltage level compatible. Could be used in conjunction with clear to send line in order to operate the 1351A, RS-232 interface at some non-standard baud rate. Clock rate must be baud rate X 16. See paragraph 2-2.

null modem is to allow two RS-232C compatible terminals to be connected. The most common example is a computer or calcuator connected to an operator terminal via a null modem device. Figure 1-3 shows a typical null modem connection on the left. On the right is the HP supplied inverter or "un-null" modem cable The purpose of the second cable is to undo the crossover effects of the first null modem.

1-5. CABLES FOR THE 1351A.

From a signal direction point of view, the 1351A appears to be a modem. This signal convention can be observed in table 1-2, figure 1-3 and in schematic 2E. However, the 1351A does not provide the signals normally associated with a modem. Functionally, it acts like a standard RS-232C terminal.

Two accessories are provided with the 1351A which allow the user to select the most convenient and functional installation.

a. A spare RS-232 female connector: This connector is for those installations where the user would like to plug the computer directly into the 1351A. The male connector on the existing computer cable is replaced with the spare female connector.

b. The HP inverter or un-null modem cable: This cable is for those installations where the user would prefer not changing the computer cable or where there is an existing null modem cable or terminal block. The purpose of the HP inverter cable is to undo or provide the signal crossovers necessary to maintain compatibilities.

In all installations,the user should refer to the information in table 1-2, figure 1-3, and schematic 2E. In addition, the user should review the signal specifications given for his communication interface line. The best self check is to draw out an inter-connect diagram similar to that shown in figure 1-3 and check both the signal directions, and the signal names (functions).

SECTION II

INSTALLATION

2-1. CONFIGURATION OPTIONS.

Before attempting to use the 1351A/Option 001, a complete understanding of your data transmission system is required. A Systems Engineer can greatly simplify this task. The 52105A I/O board can be set up for several different transmission configurations. Figure 2-1 and tables 2-1 and 2-2 provide the information you need to set up the 1351A/Option 001 in your system. The following items must be determined and the configuration of the 52105A RS-232C interface board (A3) and/or its mating cable must be changed as necessary.

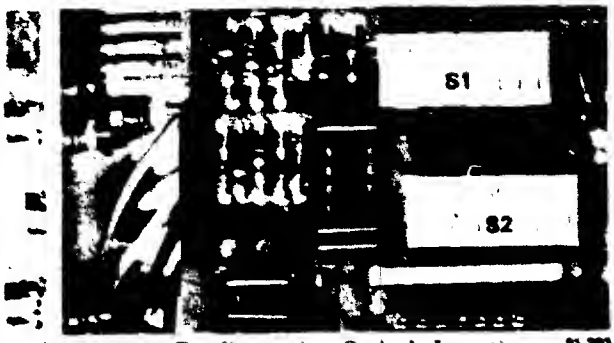


Figure 2-1. Configuration Switch Locations

Table 2-1. Configuration Switch S2 Settings

Function	Position 8 7 6 5 4 3 2 1	Factory Set
Transmit 7 Bits	1	X
Transmit 8 bits	1	F
Transmit 1 Stop Bit	2	F
Tramsmit 2 Stop Bits	2	
Transmit with Parity	3	
Transmit Without Parity	3	F
Transmit Odd Parity	4	
Transmit Even Parity	4	F
57.6 Kbaud or Ext/16	X X X X	*
50 Baud	0 X X X	
75 Baud	X 0 X X	
110 Baud	0 0 X X	
134.5 Baud	X X 0 X	
150 Baud	0 X 0 X	
300 Baud	X 0 0 X	
600 Baud	0 0 0 X	
900 Baud	X X X 0	
1200 Baud	0 X X 0	
1800 Baud	X 0 X 0	
2400 Baud	0 0 X 0	
3600 Baud	X X 0 0	
4800 Baud	0 X 0 0	
7200 Baud	X 0 0 0	
9600 Baud	0 0 0 0	F

X = Closed Position
0 = Open Position
F = Set at Factory
* = Requires use of X8 or X16 gated TTL Clock out of 52105A. See paragraph 2-6.

a. Number of character bits: Length of the data word. See table 2-1 switch S2 position 1.

b. Number of stop bits: See table 2-1 switch S2 position 2.

c. Word parity: Transmit with or without parity. See table 2-1, switch S2 position 3.

d. Type of parity: Transmit with odd or even parity. See table 2-1, switch S2 position 4.

e. Baud rate: Speed of data transmission. See table 2-1, switch S2 positions 5,6,7 and 8.

f. Signal cables and wires: RS-232C systems might be connected to a null modem so the exact pin out of the connectors must be known. See paragraph 1-4.

g. System clocking: RS-232C systems use Clear To Send and Request To Send flags to control the flow of data. However, other RS-232 systems use a gated clock for this function. Refer to paragraph 2-6 for external clocking considerations.

h. Blinking display: The 1351A can produce a blinking display via hardware control. Refer to table 2-2, switch S1 positions 6, 7 and 8. In addition, the 1351A Operating and Service Manual, Section III should be reviewed.

2-2. CIRCUIT BOARD DESCRIPTION.

The 52105A RS-232C interface for the 1351A can be set up to either the Modem or Terminal configuration as described by the RS-232C specification. In addition other RS 232 configurations can be established.

2-3. CIRCUIT BOARD RECONFIGURATION.

The 52105A RS-232C interface module is a flexible system that can accommodate most RS-232 systems presently in use. As supplied from the factory, it conforms to the RS-232C configuration for a modem. However, it can be changed to the terminal configuration or one of many external clocking configurations. The recommended procedure for modifying the configuration of the 52105A I/O board is to modify the cable connecting it to your system. However, the 52105A can be reconfigured by the addition and deletion of jumpers on the printed circuit board. This should be attempted only by qualified service personnel. Refer to schematic 2E and figures 2-2 and 2-3 for jumper functions and locations when changing the interface configuration.

Table 2-2. Configuration Switch S1 Positions

Function	Position 8 7 6 5 4 3 2 1	Factory Set
TTL Clock Connected (J-16)	X	F
TTL Clock Not Connected (J-16)	0	
Serial Data Out Connected (J-3)	X	
Serial Data Out Not Connected (J-3)	0	F
Serial Data In Connected (J-2)	X	F
Serial Data In Not Connected (J-2)	0	
Clocks Out Gated with BUSY	X	F
Clocks Out Not Gated With BUSY	0	
Don't Care	X	
Don't Care	0	F
Enable Hardware Blink Display 3	X	F
Don't Enable Hardware Blink Display 3	0	
Enable Hardware Blink Display 1	X	F
Don't Enable Hardware Blink Display 1	0	
Enable Hardware Blink Display 2	X	F
Don't Enable Hardware Blink Display 2	0	

X = Closed
0 = Open
F = Set at Factory

CAUTION

The 52105A is constructed on a four layer p.c. board and excessive heat while soldering can cause extensive damage. Soldering should only be attempted by qualified service personnel.

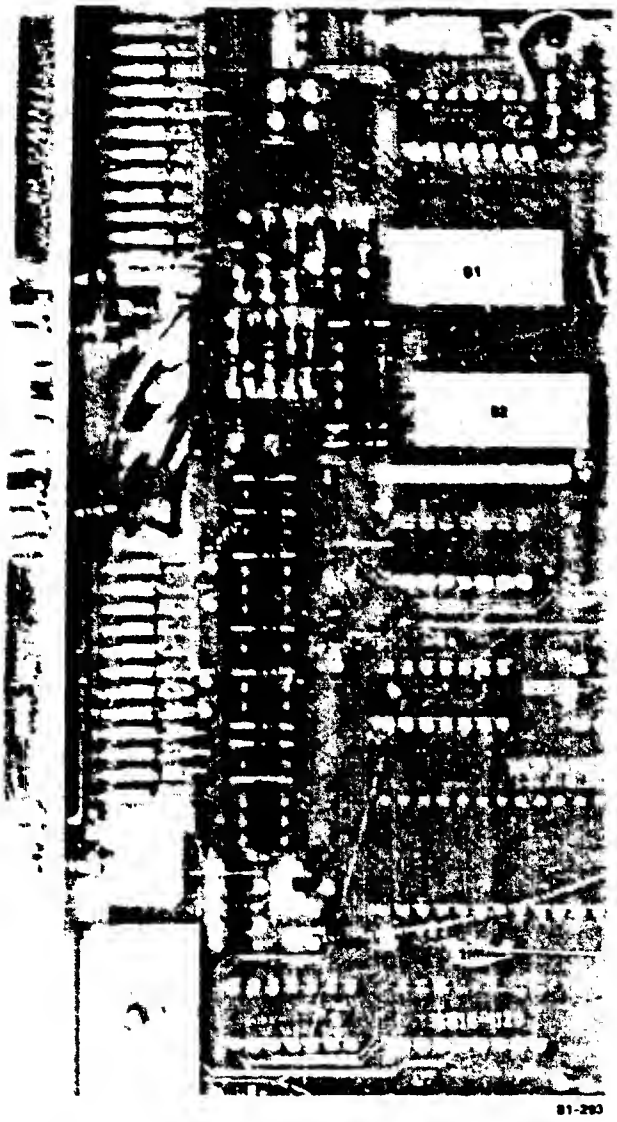


Figure 2-2. Jumper Resistor Locations (Close-up)

2-4. MODEM CONFIGURATION.

The 52105A is shipped in the modem configuration as defined by the RS-232 specification. The Modem RS-232C configuration accepts data in on pin 2 and sends data out on pin 3. To obtain this configuration, set switches S1 and jumpers as follows:

S1-2 closed
S1-3 closed
E-23 removed
E-24 removed

This configuration can be reversed by setting S1, E23 and E24 as follows:

S1-1 open
S1-3 open
E-23 installed
E-24 installed

2-5. TERMINAL CONFIGURATION. The 52105A can be changed to the terminal configuration by setting S1 and installing/removing jumpers. The terminal configuration is shown below:

Pin	Direction	Name and/or Function
2	out of 1351A	Transmitted Data
3	into 1351A	Received Data
4	out	Request To Send
5	in	Clear To Send
6	in	Data Set Ready
7	-	Signal Ground
8	in	Carrier Detector

This configuration can be obtained by setting the 52105A as follows:

Data Lines

S1-2 open
S1-3 open
E-23 installed
E-24 installed

Request To Send/Clear To Send

E7 installed
E19 open
E20 installed
E21 open
E22 installed

Carrier Detect

E31 installed
E14 open

2-6. EXTERNAL CLOCKING SYSTEMS. An external clock can be used to control the flow of data from the controller to the 1351A/Option 001 when the Clear To Send, and Request To Send flags are either unavailable or unwanted in your system. An external clock can also be used to obtain transmission Baud rates other than those available with the selection switch.

A detailed knowlege of the controllers output port is required to set up an externally clocked system. For example, the following information is needed:

a. Clock Level, TTL or RS-232
b. Clock Source, from controller or from 1351A
c. Signal input and output pins
d. If the clock level is TTL, is the clock frequency 8 times or 16 times the baud rate.

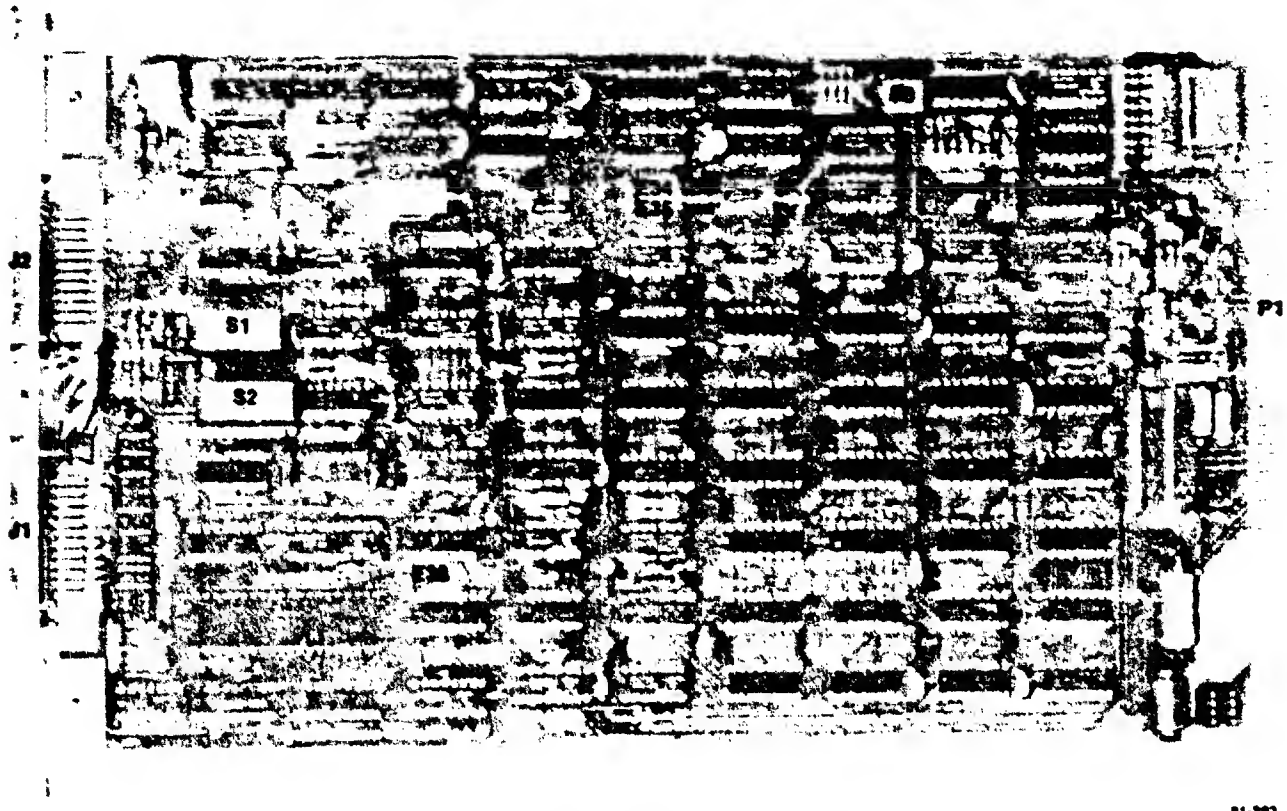


Figure 2-3. Jumper Resistor Locations (Over-all View)

Although there is no standard for externally clocked RS-232 systems,through useage a few configurations have emerged as more common. The 52105A can be configured as follows:

a. TTL Level clock from the 1351A Option 001 at either 8 or 16 times the baud rate to control the output of the controller.

b. RS-232 level clock from the 1351A Option 001 at 16 times baud rate to control the output of the controller.

c. RS-232 level clock from the controller at 16 times the baud rate to control the data loading into the 1351A Option 001.

NOTE

If the Clear To Send flag is not used in conjunction with this clock input, software delays must be use to prevent sending data to the 1351A/Option 001 when it is busy. This delay must be 2X the worst case refresh rate or 96 milliseconds for each instruction issued.

Tne 52105A circuit board contains jumper positions that allow the configuration to be set up to the needs of your system. Refer to schematic 2E and figures 2-2 and 2-3 for jumper functions and positions.

CAUTION

The 52105A is constructed on a four layer p.c. board and excessive heat while soldering can cause extensive damage. Soldering should only be attempted by qualified service personnel.

Some of the most common external clock configurations are as follows:

TTL Clock Frequency

Baud Rate X 16
- E34 = installed
- E35 = installed
- E36 = open
- E37 = open

Baud Rate X 8
- E34 = open
- E35 = open
- E36 = installed
- E37 = installed

Gated Clock Output. Both the TTL and RS-232 clock outputs can be gated with the 1351A/Option 001 Ready flag to prevent data from being transmitted when the 1351A/Option 001 is not able to receive the data.

Switch S1-4 selects this feature. If gating is disabled (S1-4 open), software delays or Clear To Send and Request To Send flags must be used to prevent writing data to the 1351A/Option 001 when it is busy. If the software delay is used, the delay time must be 2X the worst case refresh rate or 96 milliseconds for each instruction issued.

External Clock Input. The 52105A is supplied from the factory in the internal clock configuration and jumpers must be changed to allow it to receive an external RS-232 level clock on pin 24 of the I/O connector. The jumpers required are shown below. In addition, S2 positions 5 through 8 must be set as shown in table 2-2.

In this configuration, the 52105A will provide TTL and RS-232 level gated clock outputs. Either of these signals can be used to control the data output of the data source. To prevent monitoring control flags, and/or providing software delays, this configuration is recommended.

As with the gated clock output clock configuration, switch S1-4 selects this feature. If gating is disabled (S1-4 open), software delays must be added to prevent writing data to the 1351A/Option 001 when it is busy. This delay time must be 2X the worst case refresh rate or 96 milliseconds for each instruction issued.

	Internal Clock	External Clock
E11	installed	open
E12	installed	installed
E13	open	installed
E14	installed	open
E32	open	installed
E33	installed	open

2-7. HP SYSTEM 1000 JUMPER CONFIGURATION.

The System 1000's Model 12531 C-001 high speed terminal RS-232C interface card should be configured as follows:

Jumper	Position	Function
W1	B	EXT TTL CLOCK
W2-6	DON'T CARE	
W7	B	ONE STOP BIT

The 1351A-001 I/O board remains in its factory configuration.

2-8. HP SYSTEM 1000 CABLE CONFIGURATION.

The following are necessary cable connections for a System 1000/1351A Option 001 interface:

COMPUTER END:

Terminals	Wire Color	Signal
4,D,Y	Jumpered Together	
16,T,V	Jumpered Together	
L	OR	EXT TTL Clock
W	BRN	Data to Device
X	WHT	Data from Device
BB	BLK	Gnd 1
24	BLK	Gnd 2

PERIPHERAL END:

Terminal	Wire Color	Signal
1	BLK	Gnd 2
2	BRN	Data to Device
3	WHT	Data from Device
7	BLK	Gnd 1
16	OR	EXT TTL Clock

2-9. INSTALLATION AND REMOVAL.

The electrical power to the 1351A should always be removed (power switch "off" and line cord disconnected) when installing or removing the interface card (HP-IB or RS-232C). In addition, the power should be disconnected when an interface card is not installed.

For the convenience of inserting or removing the interface board, there are circuit board guides in the 1351A. If it should ever become necessary to get into the 1351A, the top and bottom covers can be removed by qualified service personnel. For safety, the power must be removed from the 1351A whenever covers are taken off.

SECTION III

PROGRAMMING CONSIDERATIONS

3-1. GENERAL PROGRAMMING CONSIDERATIONS.

The instruction set and operation of the 1351A are identical for both the HP-IB and RS-232C interfaces. Instructions and data are transmitted to the 1351A as an ASCII string message. The 1351A then assembles the string of characters into instructions based on syntax (;;cr/lf). It is therefore imperative that the character structure of the message be exact. For a review of the instruction format, refer to the "Operating and Programming Manual." Table 3-1 is a summary of 1351A instructions.

From a programming point of view there are three types of instructions:

a. Status
b. Memory Reference
c. Data (PA and TX)

The status instructions are of particular interest. Once they are issued, the status they establish is in effect until the next status instruction is issued. This feature represents a real programming advantage. Consider, for example, that th status for a given file is determined. The instructions for the name, pen condition, blanking, auxiliary bits, and character size only need to be transmitted once per change. The data for the file block can then be transmitted to the 1351A and the appropriate status bits will automatically be appended to each word in the file by the Status Register. Figure 3-1 is a programming diagram of this feature.

The last item to be covered in this section is the system time out on non-existent files. If the 1351A is sent an instruction to find a non-existant file, it will remain in the "busy" state for a few seconds and then terminate the instruction. If the user's software has a time out trap, the error can be detected and corrected with either a legal Find File or Find Location instruction.

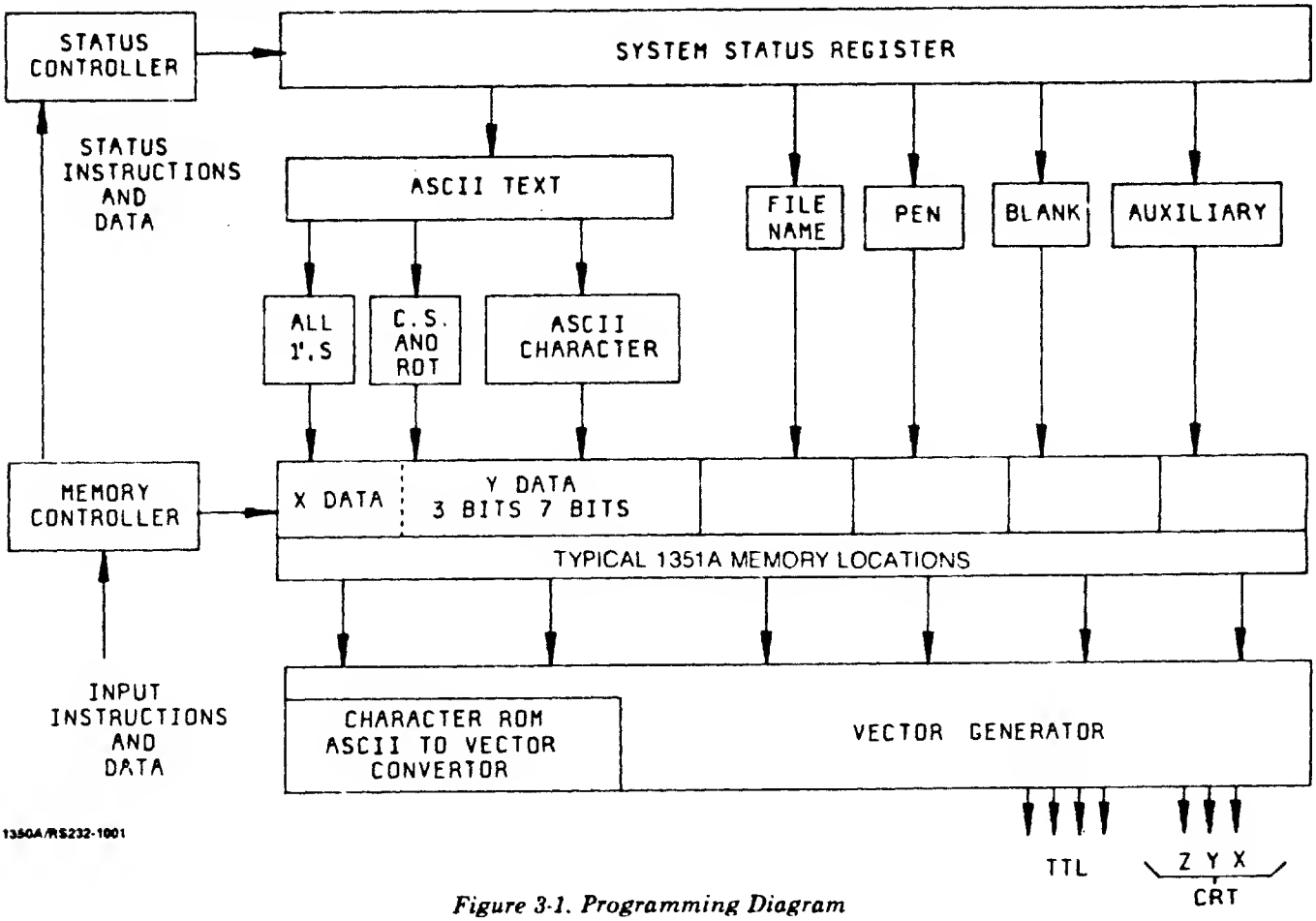


Figure 3-1. Programming Diagram

Table 3-1. 1351A Functions and Command Subsets

Function	ASCII	Commands
Initialization	EM	Erase Memory
	EN	Erase Names
	EX	Erase Auxiliary
	BM	Blank Memory
	UM	Unblank Memory
Drawing Vectors	PA	Plot Absolute
	PE	Pen Enable
Displaying Text	CS	Character Size
	TX	Text
File Operations	NF	Name File
	SN	Stop Naming
	FF	Find File
	EF	Erase File
	BF	Blank File
	UF	Unblank File
	FL	Find Location
Multiple Displays (see Chapter 5)	WX	Write Auxiliary
	SX	Stop Auxiliary

3-2. FORMATTING RULES.

a. The 1351A receives all instructions in standard ASCII code.

b. All instruction commands are two letters (ASCII) alpha characters).

c. The two-letter instruction commands may be either uppercase or lowercase. This manual will use uppercase characters.

d. All parameters are ASCII numeric characters (0 thru 9).

e. Each command consists of: (a) the two-letter command code; (b) a variable length parameter field (zero or more numerics, or a text character string); (c) a delimiter (comma [,] and possibly a semicolon [;]) following any numeric parameters; and (d) a command terminator. The command terminator may be an ASCII colon (:), or a Carriage Return character (CR), or a Line Feed character (LF).

f. Following a Text (TX) command, the 1351A must receive an ETX (End of Text) character in order to exit text mode After the ETX, the Text command must be terminated by a colon, or CR, or LF.

3-3. SYNTAX. Table 3-2 gives a dictionary of parameter ranges for the command variables used by the 1351A.

< >Angle brackets denote a syntactical variable. The user must supply a value from the specified range of possibilities given for the item.

Table 3-2. Parameter Items and Ranges

Item	Range
<abs X>	0 . . 1021
<abs Y>	0 . . 1023
<enable>	0 . . 1
<size>	0 . . 7
<location>	0 . . 8191
<file>	0 . . 63
<display>	0 . . 15
<string>	Any group of ASCII characters, excluding the ETX (End of Text) character (3 in base 10)
<end text>	ETX character
<terminator>	: or CR or LF

Table 3-3 lists 1351A command syntax. The commands are listed in alphabetical order. Spaces are used in the table to separate items within each command. For example, the command syntax for Stop Naming is indicated by "SN :" where SN is an item and the colon is an item.

In actual programming all spaces are significant and should not be entered as part of commands. The Stop Naming command would then be "SN:" only (no space between items of a command).

3-4. Command Terminators. A colon (:), Carriage Return (CR), or Line Feed (LF) character must be used to terminate each command. Table 3-3 shows a ":" (colon) as the command terminator, but remember that it may be replaced by a CR or an LF character. If both CR and LF are received (in sequence as CR/LF) the 1351A responds normally as if only one terminator was received.

NOTE

If parameter ranges are exceeded, or if formatting, syntax, and programming rules are not followed, then undesirable (and sometimes very confusing) displays can result.

Table 3-3. Command Syntax for 1351A ASCII Commands

Command Name	Syntax
Blank File	BF <file> , <terminator>
Blank Memory	BM <terminator>
Character Size	CS <size> , <terminator>
Erase File	EF <file> , <terminator>
Erase Memory	EM <terminator>
Erase Names	EN <terminator>
Erase Auxiliary	EX <terminator>
Find File	FF <file> , <terminator>
Find Location	FL <location> , <terminator>
Name File	NF <file> , <terminator>
Plot Absolute	PA <abs X> , <abs Y> ; <terminator>
Pen Enable	PE <enable> , <terminator>
Stop Naming	SN <terminator>
Stop Auxiliary	SX <terminator>
Text	TX <string> <end text> <terminator>
Unblank File	UF <file> , <terminator>
Unblank Memory	UM <terminator>
Write Auxiliary	WX <display> , <terminator>

NOTE: Each comma (,) and semicolon (;) is a required item in the command string.

3-5. PROGRAMMING RULES.

a. The 1351A follows the last Pen Enable (PE) command received (CRT beam on or off). PE can be overridden by Blank Memory (BM) or Blank File (BF) commands.

b. A Character Size (CS) command should preceed a Text (TX) command. This preconditions the size and rotation of text to be displayed. The 1351A follows the last CS command received when in text mode.

c. 1351A memory is made up of 8192 words. Each word may be either a vector endpoint coordinate pair (PAX,Y;:) or a Text character.

d. 1351A memory may be sectioned into up to 64 files. Each file can contain from one to 8192 words of memory. Total contents of all files must not exceed 1351A memory size of 8192 words.

e. A Stop Naming (SN) command should follow the last vector or character entered into a file.

f. A file, even though named, does not exist until something has been placed in it.

g. Following a command that requires a parameter a data field exists until delimited by a comma (,). This data field is of variable length. In the data field, only the last four characters will be used by the 1351A. If less than four digits are sent, the 1351A inserts leading zeroes. If more than four characters are placed in the data field (leading spaces for example), the 1351A will ignore all except the last four characters preceeding the comma. Any characters in these last four positions will be treated as digits by the 1351A.

Example:

"NFXXX...XXDDDD,:" X=don't care; D=ASCII digit

NOTE

Data fields must contain integer values only in the last four positions preceeding the comma. If computed values (for example TAN X) are done in floating point, be careful that only integer results are sent to the 1351A (truncate). No decimal point is allowed.

h. Following a PA command, the X and Y entries both follow the above rule. The X data field is delimited by a comma (,). The Y data field is delimited by a semicolon (;). The Y data field (preceeding the semicolon) follows the same rules as do the data fields that are delimited by a comma.

3-6. REQUIRED INITIALIZATION SEQUENCE. Whenever the 1351A is powered on, or whenever a new program is to be sent to the 1351A, a specific initialization sequence is required. This sequence provides the proper starting point by "clearing out" the 1351A.

If the 1351A is equipped with the HP-IB (Hewlett-Packard Interface Bus) Input/Output assembly, the Initialization should start with an Interface Clear (IFC) message from HP-IB. This message is used only with the HP-IB interface, and has no meaning for other 1351A interfaces.

The following items must be sent to the 1351A in the order given below. This insures that the 1351A will initialize properly.

1. ETX — The ASCII End of Text character (3 in base 10) makes sure that the 1351A is taken out of a possible Text mode "wake up" condition. When in Text mode, the 1351A assumes that anything received is to be displayed as characters - including command terminators and control characters.

2. DC4 — The ASCII DC4 character (20 in base 10) turns the POWER INTERRUPT indicator off. The POWER INTERRUPT indicator allows the 1351A to warn the operator if a power disruption occurs that may affect operation. POWER INTERRUPT is automatically turned on whenever the 1351A is powered on. Thus it must be turned off during initialization in order to indicate any subsequent power disruption.

NOTE

On most terminals, the ETX character can be obtained by pressing the Control [CNTL] and capital C keys at the same time. The DC4 character can be obtained by pressing [CNTL] and capital T keys at the same time.

3. : — The colon is used as a <terminator> so that the 1351A will receive the next two characters as a two-letter command. ASCII CR or LF could replace the colon (:).

4. EM: — The EM commands the 1351A to erase its memory. This "cleans out" all vector and pen enable values that are present due to the random power up of memory. The colon provides the <terminator> for the EM command.

5. EN: — The EN commands the 1351A to erase all file names present due to random memory power up. Colon terminates EN command.

6. EX: — Erases all multiple display blanking information from 1351A memory after random power up. Colon terminates EX command.

7. SN: — Stop Naming insures that no files are named until the 1351A is specifically instructed to do so. See the File Operations section of this chapter. Colon terminates SN command.

8. SX: — Stop Auxiliary insures that no data is assigned to multiple display blanking combination(s) until the 1351A is specifically instructed to do so. Multiple display blanking is covered in Section V of this manual. Colon terminates SX command.

9. UM: — Unblanks entire 1351A memory so that subsequent data to be displayed is not overridden by inadvertently having 1351A output inhibited. Colon terminates UM command.

3-7. PROTOCOLS AND PROMPTS.

The transmission of line protocols and/or user prompts (like question marks, flashing underlines, etc.) such as is found in a terminal driver, will cause operational errors in the 1351A/Option 001. The 1351A only accepts commands listed in this manual and in the Operating and Programming manual. Any others, especially those mentioned above, will "lock up" the 1351A such that it will have to be re-initialized. To minimize protocol problems, use a driver with no protocol, such as a TTY driver.

3-8. NULL AND SPECIAL CHARACTERS.

The 1351A has been designed to utilize and operate properly with only four of the special function and/or non-printing characters (note paragraph 3-4). In addition, if these control characters are used at the wrong time, an error could occur.

The following is an excellent example of how unwanted and forgotten control characters can sneak into a transmission to the 1351A. The 1351A was connected to a serial interface card on a Digital Equipment Corp. PDP-11 computer. The system was running under RSX-11M. The transmission would take place, but there was always an error in the data received by the 1351A. It was interesting that the error was always in the same place during the transmission.

The problem arose from a "special feature" which can be implemented during system generation time for buffering older terminals on the Digital Equipment Corp. computer. In essence, it amounted to sending a null character and a LF/CR after X number of ASCII characters. The purpose of the function was to allow a slower terminal to catch up on long transmissions. However, the 1351A considers this as an error.

As it turned out, this was a simple problem to correct. The output specification for the device handler was changed from QIOW$ IO.WVB to QIOW$ IO<WAL, which says "write all" (no buffering).

In general, this is the sort of error that can occur but is simple to correct once it is understood.

3-9. SPECIFIC PROGRAMMING POINTS.

From the point-of-view of a software designer, the main attributes of the 1351A are:

a. The flexible file structure

b. The speed of displaying new test data and/or graphical information

c. Selective erase and update

These features should always be kept in mind at the onset of an application. Probably the best way to describe these features is by way of a few examples.

3-10. THREE-DIMENSIONAL ROTATION. Since there are 64 definable files in the 1351A, suppose that each file contained one fiew of an object. If each view was taken in a plane through the object every 5.62 degrees, then the object would be completely described for one full rotation (360 degrees). If one file at a time is sequentially unblanked, the CRT would appear to be displaying an object rotating in 3-Dimensions.

NOTE

The important thing to realize in this example is that the file data for the object view was only transmitted once. Then the only thing that was required to rotate the object was the transmitting of the sequential blanking instructions.

3-11. HIGH SPEED FILE UPDATING. In a typical graphics application, there is usually a considerable range of requirements for updating groups of data. For instance, portions of the graphics picture are relatively fixed for various points in time (like building outline, process control flow diagrams, printed circuit boards , text,...) while other portions continuously change. For this reason, it is advantageous to group and segment the files in the 1351A to match the structure of display data in terms of function similarities and/or frequency of change. In this way, only the display segments which need to be visually changed or updated will be affected in memory. In addition, files can be given priorities for updating, buffer files can be created and displayed alternately, or only a single word can be updated.

3-12. REDUCING VISUAL FLICKER. The display refresh rate can be significantly increased by data management. In some applications, like radar, pseudo-random data is displayed. If the random data is presorted and grouped into areas on the screen, the writing beam will have more time for refreshing the data rather than spending most of its time traveling back and forth around the screen for each data point.

3-13. PROGRAMMING EXAMPLES.

The optimal method to gain understanding of the 1351A/Option 001 Graphics Translator is through actual programming experience. In order to show how to program it, a common example will be used with three different software implementations.

The example programs all draw a triangle on the CRT with "1351A" displayed below the triangle. Figure 3-2 shows the display generated by any of the example programs.

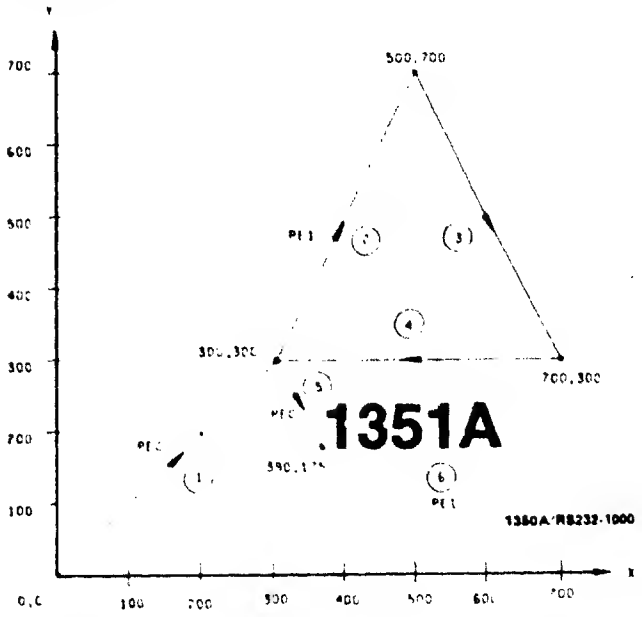


Figure 3-2. Diagram of Example Program Display

3-14. GENERAL INSTRUCTIONS. Since 1351A addressable resolution is about 1000 by 1000, let us draw the triangle in the middle of the CRT. This places the vector endpoints at (300,000), (500,700), and (700,300). The (0,0) point is at the bottom left hand corner of the CRT. Following are the general steps needed.

a. Initialize the RS-232C interface card in the computer that is controlling the 1351A.

b. Initialize the 1351A (turn off the text mode and power interrupt light).

c. Erase all the memory in the 1351A.

d. Set all auxiliary bits to zero.

e. Turn the display "on" (in software).

f. Turn the beam "off" and move it to the first point of the triangle, then turn the beam "on."

g. Place the end points for triangle in file 1, then turn "off" file 1.

h. Turn "off" the beam.

i. Move the beam to the location for the first text character, i.e. the "1" in 1351A.

j. Turn the beam "on."

k. Set the character size and rotation.

l. Place the text in file 16.

m. Turn "off" the text mode.

n. Turn "off" file 16.

o. Turn "off" the pen.

The following is a list (in order) of the instructions which must be sent to the 1351A in "ASCII":

3 in decimal (one byte) ETX
20 in decimal (one byte) DC4
13 in decimal (one byte) CR
10 in decimal (one byte) LF
em:en:ex:sn:sx:um:
nf1,:pe0,:pa300,300,:
pe1,:pa500,700;700,300;300,300;:sn:
nf16,:pe0,:pa390,175;:pe1,:
cs2,:tx1350A(ETX=3 in decimal):sn:

Blanks and random spaces are not permitted. The list of instructions shown is the ASCII string of characters which must be transmitted to the 1351A.

3-15. HEWLETT-PACKARD 9825A/HPL INSTRUCTIONS.

```
0: "CLEAR THE 1351A INTERFACE":
1: wtc 10,1;wtb 10,0;wtc 10,0
2: "set up the RS232 handshake":
3: wtc 10,1;wtb 10,37;wtc 10,0
4: "clear the 1351A":
5: wtb 10,3,20,":em:en:ex:sn:sx:um:"
6: "draw a triangle in file 1":
7: wrt 10,"nf1,:pe0,:pa300,300;:pe1,:pa500,700;700,300;300,300;:sn:"
8: "write text into file 16":
9: wrt 10,"nf16,:pe0,:pa390,175;:pe1,:"
10: wtb 10,"cs2,:tx1351",3,":sn:"
11: stp
```

3-16. HEWLETT-PACKARD SYSTEM 1000/BASIC INSTRUCTIONS.

NOTE

To operate with a 1351A/Option 001, the System 1000 requires a 12531C interface card set up for external X8 TTL clock operation. In addition, the 12531C card must be driven with driver 0.

In this case, the control functions (3,20) are obtained by using the control key and proper key.
3 = control/C = C/C = ETX
20 = control/T = C/T = DC4

```
10  REM   EXAMPLE PROGRAM FOR THE 1351A ON THE SYSTEM 1000, IN BASIC
20  REM      CLEAR THE HPIB AND 1351A INTERFACE
30  CALL CLEAR(11,2)
40  REM   SET THE ETX AND DC4 ASCII CODES
50  LET E$=" "
60  LET D$=" "
70  REM   CLEAR THE 1351A
80  PRINT  #19;E$,D$,":EM:EN:EX:SN:SX:UM:"
90  REM   DRAW THE TRIANGLE IN FILE 1
100  PRINT  #19;"NF1,:PE0,:PA300,300;:PE1,:PA500,700;700,300;300,300;:SN:"
110  REM   WRITE TEXT INTO FILE 16
120  PRINT  #19;"NF16,:PE0,:PA390,175;:PE1,:"
130  PRINT  #19;"CS2,:TX1351A:SN:"
140  STOP
150  END
```

3-17. HEWLETT-PACKARD SYSTEM 1000/FORTRAN INSTRUCTIONS.

NOTE

To operate with a 1351A/Option 001, the System 1000 requires a 12531C interface card set up for external X8 TTL clock operation. In addition, the 12531C card must be driven with driver 0.

```
0001  FTN4,L
0002  C - - - -  EXAMPLE PROGRAM FOR THE 1351A ON THE SYSTEM 1000, IN FORTRAN
0003        PROGRAM EXPLF
0004  C.....  SET THE RS232 LU to 11
0005        LRS232=11
0006  C.....  SET THE 1351A LU TO 19
0007        IPLT=19
0008  C.....  CLEAR THE RS232 BUS AND THE 1351A
0009        CALL RS232(IPLT,LRS232)
0010  C.....  DRAW A TRIANGLE INTO FILE 1
0011        WRITE(IPLT,1)
0012      1 FORMAT("NF1,:PE0,:PA300,300;:PE1,:PA500,700,700,300;300,300;:SN:")
0013  C.....  WRITE TEXT INTO FILE I6
0014  C.....    SET UP THE ETX CODE (UPPER HALF)
0015        IETX=3*256
0016        WRITE(IPLT,2) IETX
0017      2 FORMAT("NFI6,:PE0,:PA390,175;:PE1,:CS2,:TX1351A",A1,":SN:")
0018        STOP
0019        END

FTN4 COMPILER: HP92060-16092 REV. 1913 (790206)

** NO WARNINGS ** NO ERRORS **  PROGRAM = 00095      COMMON = 00000

0020  C
0021  C - - - - - - - - - - - -  RS232  - - - - - - - - - - - -
0022  C
0023  C  CLEARS THE RS232 BUS AND THE 1351A, WHERE
0024  C          IPLT      - LU OF THE 1351A
0025  C          LRS232    - LU OF THE RS232 SERIAL I/O CARD, DRIVER 0
0026  C
0027            SUBROUTINE RS232(IPLT,LRS232)
0028  C  .....  DO AN INTERFACE CLEAR TO THE CARD ITSELF
0029            CALL EXEC(3,LRS232)
0030  C  .....  SEND AN ASCII "ETX" + "DC4" AND CLEAR THE 1351A
0031  C  .....    ETX TAKES THE 1351 OUT OF TEXT MODE
0032  C  .....    DC4 CLEARS THE POWER INTERRUPT
0033            I=01400B+24B
0034            WRITE(IPLT,1) I
0035          1 FORMAT(A2,":SX:SN:EM:EN:EX:UM:PE0,:CS,:")
0036            RETURN
0037            END

FTN4 COMPILER: HP92060-16092 REV. 1913 (790206)

** NO WARNINGS ** NO ERRORS **  PROGRAM = 00045      COMMON = 00000
```

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

The procedures in this section provide an abbreviated test that provides approximately 90% assurance of proper 1351A operation.

4-2. EQUIPMENT REQUIRED.

The verification programs are written for an HP Model 9825A Calculating Controller equipped with Options: 98210A (String-Advanced Programming ROM); 98214A (9862A Plotter-General I/O-Extended I/O ROM); and 98036A Serial I/O Interface with the 98036A set to "10". The comments that accompany the programs should allow them to be translated for use with other (RS-232) controllers. The X-Y display must satisfy the critical specifications listed in table 1-1.

NOTE

The performance test programs may be put on tape. This will save time and prevent errors whenever the tests are repeated.

4-3. PERFORMANCE TEST PROCEDURES.

4-4. PERFORMANCE VERIFICATION.

4-5. BAUD RATE CHECK.

Reference:
Schematic 2E.

DESCRIPTION:
Five baud rates will be checked. It will be necessary to remove the board to set the baud rate switches for each range.

EQUIPMENT:
Oscilloscope (or Counter)..... HP1740A

PROCEDURE:

a. Turn power off before removing I/O board.

b. Remove I/O board out the back of the 1351A by unscrewing two knurled screws and pull the board straight back.

c. Set S2 to step 1 configuration shown in table 4-1.

Table 4-1. Baud Rate Configuration

STEP	S2-5	S2-6	S2-7	S2-8	PERIOD	FREQUENCY
1	Closed	Open	Open	Open	104.3 μs	9600
2	Open	Closed	Open	Open	26 μs	38.4 K
3	Open	Open	Closed	Open	13 μs	76.8 K
4	Open	Open	Open	Closed	8.7 μs	115.2 K
5	Closed	Closed	Closed	Closed	2.17 μs	460.8 K

d. Insert board, turn power on and check p in 15 of RS-232C connector for a waveform with a period or frequency listed in table 4-1. The level will be 15 V p-p.

---

e. Repeat for steps 2, 3, and 4.

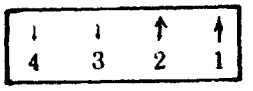
f. Set switch S2 as shown in step 5 and monitor the TTL level squarewave (+.2 to +5 V) at pin 16 of the RS-232C connector.

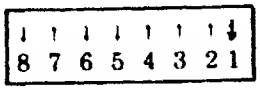
Next set switch S2-5, 6, 7, and 8 to the following positions:

S2-5	S2-6	S2-7	S2-8
Open	Open	Open	Open

This sets the buad rate to 9600 and is left there for the rest of the performance test. When the performance test is complete the switches should be returned to the desired baud rate.

To be compatible with the factory settings of the 1351A-001, the internal switches within the main body of the 98036A calculator serial interface should be set as shown.





NOTE – MANUAL UPDATE INCORPORATED

A special cable will need to be constructed (see figure 4-2).

The cable should then be marked "special 9825A/98036A to 1351A Option 001 serial interface adapter cable".

4-6. I/O OPERATIONAL VERFICATION.

The following program assumes the 98036A is set to an address of 10 (factory setting) and the baud rate switch to 1 (9600 buad).

The switches and jumpers on the 52105-66501 I/O board in the 1351A will need to be configured as shown in figure 4-1 (factory setting).

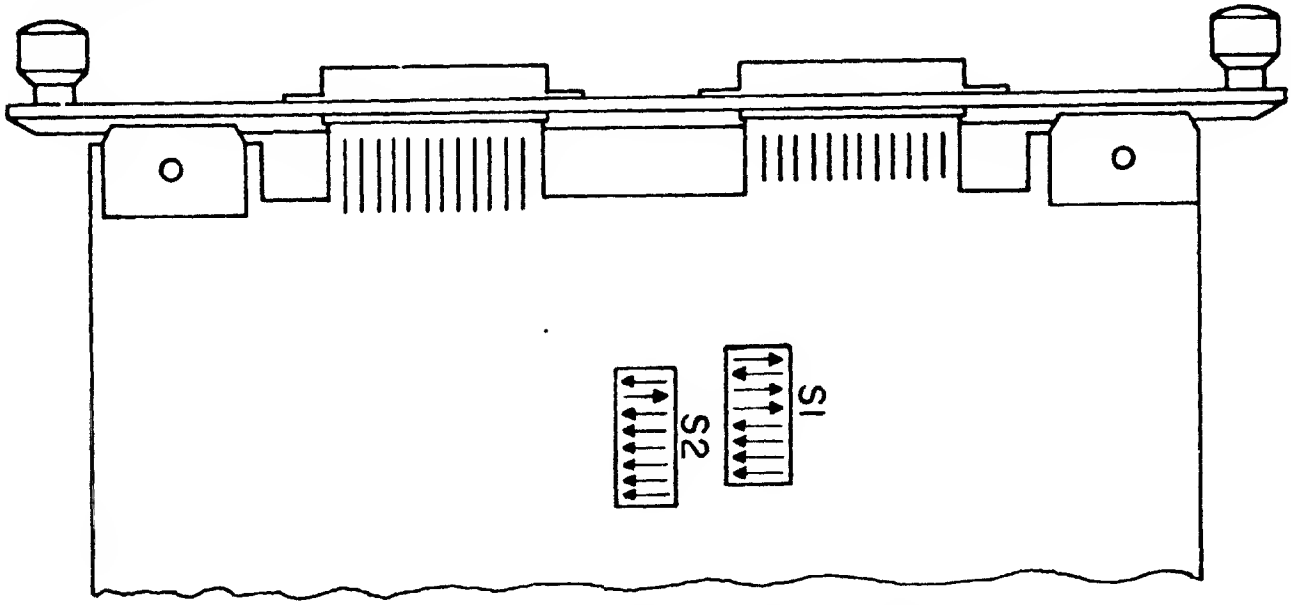


Figure 4-1. S1 and S2 Settings for Performance Tests

PERFORMANCE TESTS

DESCRIPTION:

A sequence of program steps is sent to the 1351A via RS-232-C. At appropriate points the program stops and the 1351A front panel or display CRT is checked. These program steps exercise most 1351A functions.

EQUIPMENT:

Controller ..... HP 9825A/98036A
X-Y Display ..... HP 1311A

PROCEDURE:

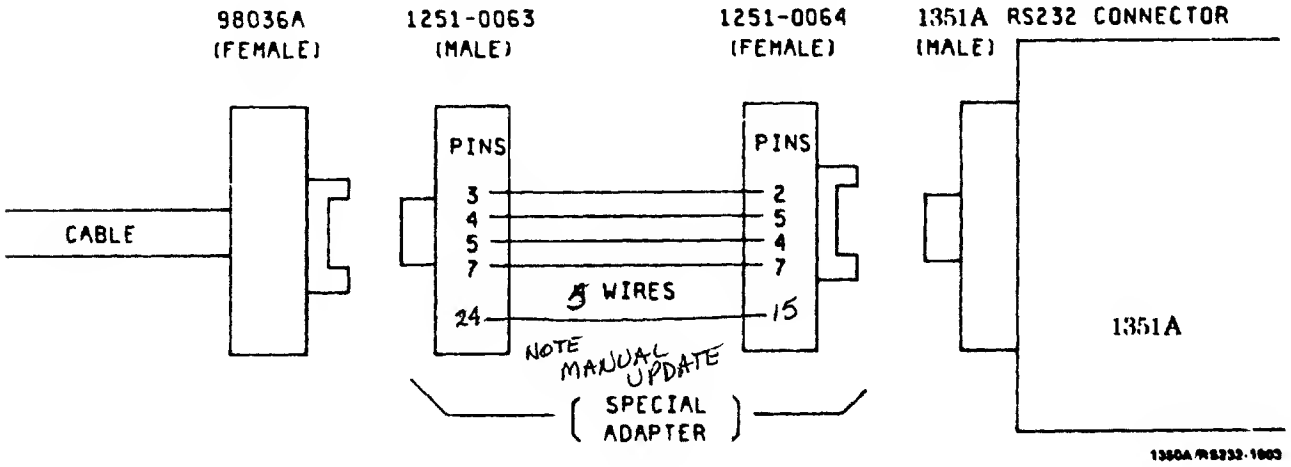


Figure 4-2. Performance Verification Test Setup

a. Connect 1351A X, Y, and Z outputs to display X, Y, and Z inputs.

b. Make sure that display is in 50-ohm input configuration. Also, make sure that display TTL blanking input has shorting cap installed on postive-going input.

c. Connect interface cable 98036A through special adapter cable to rear of 1351A. Equipment should now be as shown in figure 4-2.

d. Cycle the LINE power switches for the 9825A, the 1351A, and the X-Y display being used. Verify that random vectors are displayed by the display CRT.

e. Enter the following program on the 9825A.

```
0: wtc 10,1;wtb 10,37;wtc 10,0;wrt 10;beep;stp
1: wtb 10,"PA";beep;stp
2: wtb 10,3,20,13,10;beep;stp
3: wrt 10,"EM";beep;stp
4: wrt 10,"EM::EN::EX::SN::SX::UM::"
5: wrt 10,"PE1,:PA1020,1020;";beep;stp
6: wrt 10,"EM::EN::EX::SN::SX::UM::"
7: wtb 10,"PE0,:PA400,300;:PE1,:CS0,:TXB",3,13,10
8: wtb 10,"CS7,:TX S",3,13,10;beep;stp
9: wrt 10,"EM::EN::EX::SN::SX::UM::"
10: wrt 10,"NF0,:PE1,:PA800,300;:SN"
11: wrt 10,"NF31,:PA100,800;:SN";beep;stp
12: wrt 10,"BF0,";wait 1000;wrt 10,"BF31,";beep;stp
13: wrt 10,"EN::UF0,";beep;stp
14: wrt 10,"BM";wait 1000;wrt 10,"UM";beep
15: dsp "That's all FOLKS!!";wait 500;gto 14
16: end
```

f. Press 9825A RUN key. 9825A should make a "beep" sound. Verify that 1351A front-panel "LISTEN PROGRAM" LED is on.

Line 0: Initializes Interface

g. Press 9825A CONTINUE key. 9825A should beep. Verify that 1351A "LISTEN DATA" LED is on, "PROGRAM" LED is off.

line 1: wtb 10,"PA"; addresses 1351A to "listen" and sends two "program" instruction bytes without a terminating ";" (colon) or CR (Carriage Return) or LF (Line Feed). This fools the 1351A into staying in "listen for data".

h. Press 9825A CONTINUE key. Verify that 1351A POWER INTERRUPT LED has been turned off. ("PROGRAM" LED will be on.)

line 2: 3 (base 10) = ASCII ETX (End of Text) value in decimal.
This insures that the 1351A is not in Text mode.
20 = ASCII DC4 character to turn off POWER INTERRUPT.
13 = ASCII CR (Carriage Return) character.
10 = ASCII LF (Line Feed) character.

i. Press 9825A CONTINUE key. Verify that CRT is now blank.

line 3: "EM" erases Pen Enable and vector values from 1351A memory following random power-up.

j. Press 9825A CONTINUE key. Verify that CRT displays a diagonal vector from lower left corner to upper right corner.

line 4: initializes 1351A.
line 5: turns beam on and causes 1351A to draw the vector.

k. Press 9825A CONTINUE key. Verify that the vector is no longer displayed. Verify that the CRT displays a small "B" (not rotated) and a large "S" (rotated 90 degrees).

line 6: initializes 1351A (removes vector).
line 7: blanks beam while it is positioned; sets character size and rotation; unblanks beam; instructs 1351A to output a "B". (Note: 3 = ETX, 13 = CR, 10 = LF).
line 8: changes character size and rotation; instructs 1351A to output a " S" (space-S).

l. Press 9825A CONTINUE key. Verify that the CRT displays two vectors that are roughly a ">" shape.

line 9: initializes 1351A (removes text).
line 10: places the bottom vector in File "0".
line 11: places the top vector in File "31".

m. Press 9825A CONTINUE key. Verify that the bottom vector is blanked first, and the top vector is blanked about one second afterward.

line 12: blanks contents of File "0" (bottom vector); waits about one second and then blanks the contents of File "31" (top vector).

n. Press 9825A CONTINUE key. Verify that both vectors are now displayed (">" pattern).

line 13: erases all file names so that all vectors are defaulted to File '0'. Unblanks File "0" to display all vectors in 1351A memory.

o. Press 9825A CONTINUE key. Verify that ">" flashes on the CRT. The 9825A should display "That's all FOLKS!!" and beep periodically.

line 14: blanks 1351A memory to inhibit CRT; waits about one second; unblanks 1351A memory to enable CRT.
line 15: really not necessary. To get out of the loop, press 9825A STOP key. The "gto 14" causes CRT vector presentation to flash.

PERFORMANCE TESTS

4-7. AUXILIARY (COLOR) VERIFICATION.

DESCRIPTION:

The following program is provided to quickly check 1351A color interface outputs when used with an HP 1338A Tri-color display. It should be used as an addition to the Performance Verification procedure shown above.

EQUIPMENT:

Controller ..... HP 9825A/98036A
Tri-color Display ..... HP 1338A

PROCEDURE:

a. Connect Auxiliary cable from 1338A to rear of 1351A.

b. Connect interface cable from 9825A to 1351A using special adapter of figure 4-2.

c. Connect 1351A X, Y, and Z to 1338A.

d. Make sure that 1338A X, Y, and Z inputs are in 50 ohm configuration.

e. Press 9825A [ERASE][a][EXECUTE] keys, if necessary, to clear 9825A memory. Enter the following program in the 9825A.

```
0: wtc 10,1; wtb 10, 37; wtc 10,0
1: wtb 10,3,20,13,10,"EM::EN::EX::SN::SX::UM::"
2: wrt 10,"NF1,:PE1,:PA1000,1000;:SN::"
3: wrt 10,"NF16,:PE1,:PA1000,0;:SN::"
4: wrt 10,"NF40,:PE1,:PA0,1000;:SN::"
5: end
```

f. Press 9825A RUN key. Verify that 1338A displays: (1) a green vector from lower left corner to upper right corner; (2) a yellow vector from upper right to lower right corners; and (3) a red vector from lower right corner to upper left corner.

line 0: initializes 98036A Interface.
line 1: initializes 1351A
line 2: uses File "1" to create the green vector.
line 3: uses File "16" to create the yellow vector.
line 4: uses File "40" to create the red vector.

SECTION V
ADJUSTMENTS

Adjustments for the Model 1351A/Option 001 (52105A) RS-232C interface are the same as those for the standard instrument. Refer to Section V in the 1351A Operating and Service Manual for complete adjustment procedures.

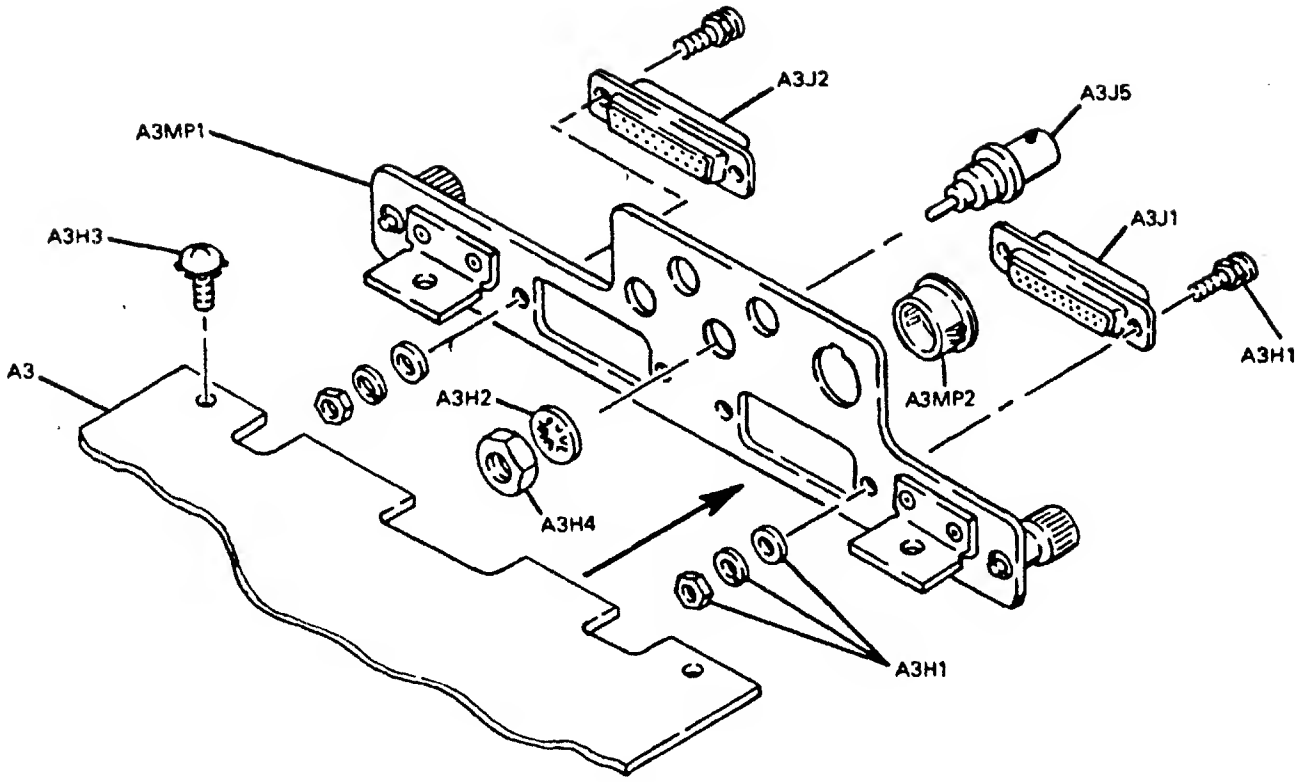


Figure 6-1. Board Assy Identification

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturer's code numbers. Figure 6-1 shows the illustrated parts breakdown.

6-2. ABBREVIATIONS.

Table 6-1 lists abbreviations used in the parts list, the schematics, and throughout the manual. In some cases, two forms of the abbreviations are used: one in all capital letters and one partial or no capitals. This occurs because the abbreviations in the parts list are always in capitals. However, in other parts of the manual other abbreviation forms are used with both lowercase and uppercase letters.

6-3. REPLACEABLE PARTS LIST.

Table 6-2 is the list of replaceable parts and is organized as follows:

a. Electrical assemblies in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

c. Electrical assemblies and their components in alphanumerical order by reference designation.

The information given for each part consists of the following:

a. The Hewlett-Packard part number and check digit.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A typical manufacturer of the part in a five-digit code.

e. The manufacturer's number for the part.

The total quantity for each part is given only once - at the first appearance of the part number in the list.

6-4. ORDERING INFORMATION.

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, indicate the quantity required and address the order to the nearest Hewlett-Packard Sales/Service Office.

To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

6-5. SPARE PARTS KIT.

Stocking spare parts for an instrument is often done to ensure quick return to service after a mualfunction occurs. Hewlett-Packard has a Spare Parts Kit available for this purpose. The kit consists of selected replaceable assemblies and components for this instrument. The contents of the kit and the Recommended Spares List are based on failure reports and repair data, and parts support for one year. A recommended Spares List for this instrument may be obtained on request and the Spare Parts Kits may be ordered through your nearest Hewlett-Packard office.

6-6. DIRECT MAIL ORDER SYSTEM.

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices.

To provide these advantages, a check or money order must accompany each order.

Mail order forms and specific ordering information is available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	assembly	F	fuse	MP	mechanical part	U	integrated circuit
B	motor	FL	filter	P	plug	V	vacuum tube neon bulb photocell etc
BT	battery	IC	integrated circuit	Q	transistor		
C	capacitor	J	jack	R	resistor	VR	voltage regulator
CP	coupler	K	relay	RT	thermistor	W	cable
CR	diode	L	inductor	S	switch	X	socket
DL	delay line	LS	loud speaker	T	transformer	Y	crystal
DS	device signaling (lamp)	M	meter	TB	terminal board	Z	tuned cavity network
E	misc electronic part	MK	microphone	TP	test point		

ABBREVIATIONS

A	amperes	H	henries	N/O	normally open	RMO	rack mount only
AFC	automatic frequency control	HDW	hardware	NOM	nominal	RMS	root-mean square
AMPL	amplifier	HEX	hexagonal	NPO	negative positive zero (zero temperature coefficient)	RWV	reverse working voltage
BFO	beat frequency oscillator	HG	mercury				
BE CU	beryllium copper	HR	hours				
BH	binder head	HZ	hertz	NPN	negative-positive negative	S-B	slow-blow
BP	bandpass					SCR	screw
BRS	brass	IF	intermediate freq	NRFR	not recommended for field replacement	SE	selenium
BWO	backward wave oscillator	IMPG	impregnated	NSR	not separately replaceable	SECT	section(s)
		INCD	incandescent			SEMICON	semiconductor
CCW	counter-clockwise	INCL	includes			SI	silicon
CER	ceramic	INS	insulation(ed)	OBD	order by description	SIL	silver
CMO	cabinet mount only	INT	internal	OH	oval head	SL	slide
COEF	coefficient			OX	oxide	SPG	spring
COM	common	K	kilo 1000			SPL	special
COMP	composition					SST	stainless steel
COMPL	complete	LH	left hand	P	peak	SR	split ring
CONN	connector	LIN	linear taper	PC	printed circuit	STL	steel
CP	cadmium plate	LK WASH	lock washer	PF	picofarads 10^{-12} farads	TA	tantalum
CRT	cathode-ray tube	LOG	logarithmic taper			TD	time delay
CW	clockwise	LPF	low pass filter	PH BRZ	phosphor bronze	TGL	toggle
				PHL	philips	THD	thread
DEPC	deposited carbon	M	milli 10^{-3}	PIV	peak inverse voltage	TI	titanium
DR	drive	MEG	meg 10^{6}	PNP	positive-negative-positive	TOL	tolerance
		MET FLM	metal film			TRIM	trimmer
ELECT	electrolytic	MET OX	metallic oxide	P/O	part of	TWT	traveling wave tube
ENCAP	encapsulated	MFR	manufacturer	POLY	polystyrene		
EXT	external	MHZ	mega hertz	PORC	porcelain	U	micro 10^{-6}
		MINAT	miniature	POS	position(s)		
F	farads	MOM	momentary	POT	potentiometer	VAR	variable
FH	flat head	MOS	metal oxide substrate	PP	peak-to-peak	VDCW	dc working volts
FIL H	fillister head	MTG	mounting	PT	point		
FXD	fixed	MY	mylar	PWV	peak working voltage	W/	with
						W	watts
G	giga 10^{9}	N	nano 10^{-9}	RECT	rectifier	WIV	working inverse voltage
GE	germanium	N/C	normally closed	RF	radio frequency		
GL	glass	NE	neon	RH	round head or right hand	WW	wirewound
GRD	grounded	NI PL	nickel plate			W/O	without

Table 6-2. Replaceable Parts

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	52105 66501	6	1	I O BOARD ASSEMBLY OPT 001	28480	52105 66501
A3C1				NOT ASSIGNED		
A3C2	0160 2201	7	7	CAPACITOR FXD 51PF ±5% 300VDC MICA	28480	0160 2201
A3C3				NOT ASSIGNED		
A3C4	0160 2201	7		CAPACITOR FXD 51PF ±5% 300VDC MICA	28480	0160 2201
A3C5	0160 2201	7		CAPACITOR FXD 51PF ±5% 300VDC MICA	28480	0160 2201
A3C6	0160 2201	7		CAPACITOR FXD 51PF ±5% 300VDC MICA	28480	0160 2201
A3C7	0160 2201	7		CAPACITOR FXD 51PF ±5% 300VDC MICA	28480	0160 2201
A3C8	0160 2201	7		CAPACITOR FXD 51PF ±5% 300VDC MICA	28480	0160 2201
A3C9	0140 0220	4	1	CAPACITOR FXD 200PF ±1% 300 VDC MICA	72136	DM15F201F0300WVICR
A3C10	0160 2055	9	29	CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C11	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C12	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C13	0180 0161	6	3	CAPACITOR FXD 3.3µF ±10% 35VDC TA	00808	T1108335K035AS
A3C14	0180 0161	6		CAPACITOR FXD 3.3µF ±10% 35VDC TA	00808	T1108335K035AS
A3C15	0160 3768	3	1	CAPACITOR FXD .01µF ±10% 100VDC CER	28480	0160 3768
A3C16	0160 2197	0	2	CAPACITOR FXD 10PF ±5% 300VDC MICA	28480	0160 2197
A3C17	0180 0161	6		CAPACITOR FXD 3.3µF ±10% 35VDC TA	00808	T1108335K035AS
A3C18	0180 0228	6	3	CAPACITOR FXD 22µF ±10% 15VDC TA	56289	150D226X9015B2
A3C19	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C20	0180 0228	6		CAPACITOR FXD 22µF ±10% 15VDC TA	56289	150D226X9015B2
A3C21	0180 1714	7	2	CAPACITOR FXD 330µF ±10% 6VDC TA	56289	150D337X9006S2
A3C22	0180 1714	7		CAPACITOR FXD 330µF ±10% 6VDC TA	56289	150D337X9006S2
A3C23	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C24	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C25	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C26	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C27	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C28	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C29	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C30	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C31	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C32	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C33	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C34	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C35				NOT ASSIGNED		
A3C36	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C37	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C38	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C39	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C40	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C41	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C42	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C43	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C44	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C45	0160 0153	4		CAPACITOR FXD 1000PF ±10% 200VDC POLYE	28480	0160 0153
A3C46	0160 2201	7		CAPACITOR FXD 51PF ±5% 300VDC MICA	28480	0160 2201
A3C47				NOT ASSIGNED		
A3C48				NOT ASSIGNED		
A3C49				NOT ASSIGNED		
A3C50	0160 0939	4	3	CAPACITOR FXD 430PF ±5% 300VDC MICA	28480	0160 0939
A3C51	0160 0939	4		CAPACITOR FXD 430PF ±5% 300VDC MICA	28480	0160 0939
A3C52	0160 0939	4		CAPACITOR FXD 430PF ±5% 300VDC MICA	28480	0160 0939
A3C53	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C54	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C55	0180 0228	6		CAPACITOR FXD 22µF ±10% 15VDC TA	56289	150D226X9015B2
A3C56	0160 2197	0		CAPACITOR FXD 10PF ±5% 300VDC MICA	28480	0160 2197
A3C57	0160 0153	4		CAPACITOR FXD 1000PF ±10% 200VDC POLYE	28480	0160 0153
A3C58	0180 0197	8		CAPACITOR FXD 2.2µF ±10% 20VDC TA	56289	150D225X9020A2
A3C59	0180 1746	5		CAPACITOR FXD 15µF ±10% 20VDC TA	56289	150D156X9020B2
A3C60	0180 1746	5		CAPACITOR FXD 15µF ±10% 20VDC TA	56289	150D156X9020B2
A3C61	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3C62	0160 2055	9		CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3CR1	1901 0040	1	6	DIODE SWITCHING 30V 50MA 2NS DO 35	28480	1901 0040
A3CR2	1901 0040	1		DIODE SWITCHING 30V 50MA 2NS DO 35	28480	1901 0040
A3CR3	1901 0040	1		DIODE SWITCHING 30V 50MA 2NS DO 35	28480	1901 0040
A3CR4	1901 0040	1		DIODE SWITCHING 30V 50MA 2NS DO 35	28480	1901 0040
A3CR5	1901 0040	1		DIODE SWITCHING 30V 50MA 2NS DO 35	28480	1901 0040
A3CR6	1901 0040	1		DIODE SWITCHING 30V 50MA 2NS DO 35	28480	1901 0040
A3E1	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E2	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E3	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E4	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E5	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3E6	1258-0124	7	NA	PIN PROGRAM JUMPER	28480	1258-0124
A3E7	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E8	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E9	1258-0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E10	1258-0124	7	NA	PIN PROGRAM JUMPER	28480	1258-0124
A3E11	1258-0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E12	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258-0124
A3E13	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E14	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E15	1258-0124	7	NA	PIN PROGRAM JUMPER	28480	1258-0124
A3E16	0684 1031	9	NA	RESISTOR 10K 10% 25W FC TC -400 +700	01121	CB1031
A3E17	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E18	1258-0124	7	NA	PIN PROGRAM JUMPER	28480	1258-0124
A3E19	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258-0124
A3E20	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E21	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E22	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E23	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E24	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258-0124
A3E25	0684 1001	3	NA	RESISTOR 10 10% 25W FC TC- 400 +500	01121	CB1001
A3E26	0160 2055	9	NA	CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3E27	0684 1001	3	NA	RESISTOR 10 10% 25W FC TC- 400 +500	01121	CB1001
A3E28	0160 2055	9	NA	CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3E29	0684 1001	3	NA	RESISTOR 10 10% 25W FC TC -400 +500	01121	CB1001
A3E30	0160 2055	9	NA	CAPACITOR FXD .01µF +80 20% 100VDC CER	28480	0160 2055
A3E31	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258-0124
A3E32	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E33	1258 0124	7	NA	PIN PROGRAM JUMPER	28480	1258 0124
A3E34	0160 2207	3	NA	CAPACITOR FXD 300PF +5% 300VDC MICA	28480	0160 2207
A3E35	0757 0283	8	NA	RESISTOR 2K 1% 125W FTC +0+100	24546	C4 1 8 TO 2001 F
A3E36	0757 0283	6	NA	RESISTOR 2K 1% 125W FTC +0+100	24546	C4 1 8 TO 2001 F
A3E37	0160 2207	3	NA	CAPACITOR FXD 300PF +5% 300VDC MICA	28480	0160 2207
A3E38	0684 1001	3	NA	RESISTOR 10 10% 25W FC TC 400 +500	01121	CB1001
A3H1	1251 0218	6	4	LOCK SUBMIN D CONN	28480	1751 0218
A3H2	2190 0016	3	4	WASHER LK INTL T 3 8 IN .377 IN ID	28480	2190 0016
A3H3	2360 0113	2	2	SCREW MACH 6 32 .25 IN LG PAN HD POZI	00000	ORDER BY DESCRIPTION
A3H4	2950 0001	8	4	NUT HEX DBL CHAM 3 8 32 THD .094 IN THK	00000	ORDER BY DESCRIPTION
A3J1	1251 5410	0	1	CONNECTOR 25 PIN M D SUBMINIATURE	28480	1251 5410
A3J2	1251 5409	7	1	CONNECTOR 25 PIN F D SUBMINIATURE	28480	1251 5409
A3J3	1250 0083	1	4	CONNECTOR RF BNC FEM SGL HOLE FR 50 OHM	28480	1250 0083
A3J4	1250 0083	1		CONNECTOR RF BNC FEM SGL HOLE FR 50 OHM	28480	1250 0083
A3J5	1250 0083	1		CONNECTOR RF BNC FEM SGL HOLE FR 50 OHM	28480	1250 0083
A3J6	1250 0083	1		CONNECTOR RF BNC FEM SGL HOLE FR 50 OHM	28480	1250 0083
A3L1	9100 3139	6	1	INDUCTOR 76µH 15% BOX 875LG	28480	9100 3139
A3MP1	82106 00301	2	1	DOOR PC	28480	82102 00301
A3MP2	0690 0024	0	1	PLUG HOLE FL HD FOR .688 0 HOLE NYL	28480	8960 0024
A3Q1	1854 0071	7	8	TRANSISTOR NPN SI PD 300MW FT 200MHZ	28480	1854 0071
A3Q2	1854 0071	7		TRANSISTOR NPN SI PD 300MW FT 200MHZ	28480	1854 0071
A3Q3	1854 0071	7		TRANSISTOR NPN SI PD 300MW FT 200MHZ	28480	1854 0071
A3Q4	1854 0071	7		TRANSISTOR NPN SI PD 300MW FT 200MHZ	28480	1854 0071
A3Q5	1854 0071	7		TRANSISTOR NPN SI PD 300MW FT 200MHZ	28480	1854 0071
A3Q6	1855 0367	6	1	TRANSISTOR UJT P ON N	28480	1855 0367
A3Q7	1854 0071	7		TRANSISTOR NPN SI PD 300MW FT 200MHZ	28480	1854 0071
A3R1				NOT ASSIGNED		
A3R2	0683 4715	0	5	RESISTOR 470 5% 25W FC TC 400 +600	01121	CB4716
A3R3	0683 4715	0		RESISTOR 470 5% 25W FC TC 400 +600	01121	CB4715
A3R4	0683 4715	0		RESISTOR 470 5% 25W FC TC 400 +600	01121	CB4715
A3R5	0683 4715	0		RESISTOR 470 5% 25W FC TC- 400 +600	01121	CB4715
A3R6	0683 2225	3	9	RESISTOR 2 2K 5% 25W FC TC -400 +700	01121	CB2225
A3R7	0683 2225	3		RESISTOR 2 2K 5% 25W FC TC 400 +700	01121	CB2225
A3R8	0683 2225	3		RESISTOR 2 2K 5% 25W FC TC 400 +700	01121	CB2225
A3R9	0683 2225	3		RESISTOR 2 2K 5% 25W FC TC 400 +700	01121	CB2225
A3R10	0683 2226	3		RESISTOR 2 2K 5% 25W FC TC- 400 +700	01121	CB2225
A3R11	0683 2225	3		RESISTOR 2 2K 5% 25W FC TC- 400 +700	01121	CB2225
A3R12	0683 2225	3		RESISTOR 2 2K 5% 25W FC TC 400 +700	01121	CB2225
A3R13	0683 2225	3		RESISTOR 2 2K 5% 25W FC TC 400 +700	01121	CB2225
A3R14	0684 4731	2	4	RESISTOR 47K 10% 25W FC TC -400 +800	01121	CB4731
A3R15	0684 1811	3	6	RESISTOR 180 10% 25W FC TC -400 +600	01121	CB1811
A3R16	0684 4731	2		RESISTOR 47K 10% 25W FC TC -400 +800	01121	CB4731
A3R17	0684 1811	3		RESISTOR 180 10% 25W FC TC -400 +600	01121	CB1811
A3R18	0683 2725	8		RESISTOR 2 7K 5% 25W FC TC- 400 +700	01121	CB2725
A3R19	0683 2225	3		RESISTOR 2 2K 5% 25W FC TC -400 +700	01121	CB2225
A3R20	0683 2725	8		RESISTOR 2 7K 5 % 25W FC TC -400 +700	01121	CB2725

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3R21	0683 2225	3		RESISTOR 2.2K 5% .25W FC TC -400 +700	01121	CB2225
A3R22	0684 1001	3	10	RESISTOR 10 10% .25W FC TC -400 +500	01121	CB1001
A3R23	0684 1001	3		RESISTOR 10 10% .25W FC TC -400 +500	01121	CB1001
A3R24	0684 1001	3		RESISTOR 10 10% .25W FC TC -400 +500	01121	CB1001
A3R25	0684 1001	3		RESISTOR 10 10% .25W FC TC -400 +500	01121	CB1001
A3R26	0684 1001	3		RESISTOR 10 10% .25W FC TC -400 +500	01121	CB1001
A3R27	0684 1001	3		RESISTOR 10 10% .25W FC TC -400 +500	01121	CB1001
A3R28	0684 1001	3		RESISTOR 10 10% .25W FC TC -400 +500	01121	CB1001
A3R29	0683 4715	0		RESISTOR 470 5% .25W FC TC -400 +600	01121	CB4715
A3R30	0684 1021	7	6	RESISTOR 1K 10% .25W FC TC -400 +600	01121	CB1021
A3R31	0684 1021	7		RESISTOR 1K 10% .25W FC TC -400 +600	01121	CB1021
A3R32	0684 1001	3		RESISTOR 10 10% .25W FC TC -400 +500	01121	CB1001
A3R33	0683 1045	3	4	RESISTOR 100K 5% .25W FC TC -400 +800	01121	CB1045
A3R34	0683 1045	3		RESISTOR 100K 5% .25W FC TC -400 +800	01121	CB1045
A3R35	0684 1011	5	2	RESISTOR 100 10% .25W FC TC -400 +500	01121	CB1011
A3R36	0684 4731	2		RESISTOR 47K 10% .25W FC TC -400 +800	01121	CB4731
A3R37	0684 1811	3		RESISTOR 180 10% .25W FC TC -400 +600	01121	CB1811
A3R38	0684 4721	0	4	RESISTOR 4.7K 10% .25W FC TC -400 +700	01121	CB4721
A3R39	0684 4721	0		RESISTOR 4.7K 10% .25W FC TC -400 +700	01121	CB4721
A3R40	0684 4721	0		RESISTOR 4.7K 10% .25W FC TC -400 +700	01121	CB4721
A3R41	0684 4721	0		RESISTOR 4.7K 10% .25W FC TC -400 +700	01121	CB4721
A3R42	0684 1021	7		RESISTOR 1K 10% .25W FC TC -400 +600	01121	CB1021
A3R43	2100 3214	0	1	RESISTOR TRMR 100K 10% C TOP ADJ 1 TRN	28480	2100 3214
A3R44	0683 1045	3		RESISTOR 100K 5% .25W FC TC -400 +800	01121	CB1045
A3R45	0683 1045	3		RESISTOR 100K 5% .25W FC TC -400 +800	01121	CB1045
A3R46	0684 1001	3		RESISTOR 10 10% .25W FC TC -400 +500	01121	CB1001
A3R47	0683 2725	8		RESISTOR 2.7K 5% .25W FC TC -400 +700	01121	CB2725
A3R48	0683 2225	3		RESISTOR 2.2K 5% .25W FC TC -400 +700	01121	CB2225
A3R49	0684 1031	9	3	RESISTOR 10K 10% .25W FC TC -400 +700	01121	CB1031
A3R50	0684 1001	3		RESISTOR 10 10% .25W FC TC -400 +500	01121	CB1001
A3R51				NOT ASSIGNED		
A3R52				NOT ASSIGNED		
A3R53	0684 1011	5		RESISTOR 100 10% .25W FC TC -400 +500	01121	CB1011
A3R54	0683 2725	8		RESISTOR 2.7K 5% .25W FC TC -400 +700	01121	CB2725
A3R55	0683 2225	3		RESISTOR 2.2K 5% .25W FC TC -400 +700	01121	CB2225
A3R56				NOT ASSIGNED		
A3R57				NOT ASSIGNED		
A3R58				NOT ASSIGNED		
A3R59				NOT ASSIGNED		
A3R60	0687 4701	2		RESISTOR 4.7 10% .5W CC TC 0-412	01121	EB4701
A3R61	0684 1031	9		RESISTOR 10K 10% .25W FC TC -400 +700	01121	CB1031
A3R62	0757 0489	0	1	RESISTOR 150K 1% .125W F TC 0+100	28480	0757-0489
A3R63	0684 1021	7		RESISTOR 1K 10% .25W FC TC -400 +600	01121	CB1021
A3R64	0684 1811	3		RESISTOR 180 10% .25W FC TC -400 +600	01121	CB1811
A3R65	0684 2211	9	1	RESISTOR 220 10% .25W FC TC -400 +600	01121	CB2211
A3R66	0684 1811	3		RESISTOR 180 10% .25W FC TC -400 +600	01121	CB1811
A3R67	0757 0488	3	1	RESISTOR 909K 1% .125W F TC 0+100	28480	0757-0488
A3R68	0684 1031	9		RESISTOR 10K 10% .25W FC TC -400 +700	01121	CB1031
A3R69	0684 1021	7		RESISTOR 1K 10% .25W FC TC -400 +600	01121	CB1021
A3R70	0684 1021	7		RESISTOR 1K 10% .25W FC TC -400 +600	01121	CB1021
A3R71	0684 4731	2		RESISTOR 47K 10% .25W FC TC -400 +800	01121	CB4731
A3R72	0684 1811	3		RESISTOR 180 10% .25W FC TC -400 +600	01121	CB1811
A3R73	0683 2725	8		RESISTOR 2.7K 5% .25W FC TC -400 +700	01121	CB2725
A3R74	0683 2225	3		RESISTOR 2.2K 5% .25W FC TC -400 +700	01121	CB2225
A3R75	1810 0275	1	1	NETWORK RES 10 SIP 10K OHM 9	01121	210A102
A3S1	3101 2094	5	2	SWITCH RKR DIP RKR ASSY 8 1A 05A 30VDC	28480	3101 2094
A3S2	3101 2094	5		SWITCH RKR DIP RKR ASSY 8 1A 05A 30VDC	28480	3101 2094
A3S3	3101 2348	1	1	SPDT SWITCH	28480	3101 2348
A3U1	1820 1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74AN
A3U2				NOT ASSIGNED		
A3U3				NOT ASSIGNED		
A3U4				NOT ASSIGNED		
A3U5				NOT ASSIGNED		
A3U6				NOT ASSIGNED		
A3U7	1816 1120	9	1	IC TTL S 1K ROM SD NS O C	18324	N82S126F PROGRAMMED
A3U8	1820 1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74AN
A3U9	1820 1201	6	5	IC GATE TTL LS AND QUAD 2 INP	01295	SN74LS08N
A3U10	1820 1199	1	3	IC INV TTL TS HEX 1 INP	01295	SN74LS04N
A3U11				NOT ASSIGNED		
A3U12				NOT ASSIGNED		
A3U13				NOT ASSIGNED		
A3U14	1820 1216	3	1	IC DCDR TTL LS 3 TO 8 LINE 3 INP	01295	SN74LS138N
A3U15	1820 1203	8	3	IC GATE TTL LS AND TPL 3 INP	01295	SN74LS11N
A3U16	1820 1197	9	2	IC GATE TTL LS NAND QUAD 2 INP	01295	SN74LS00N
A3U17	1820 1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74AN
A3U18				NOT ASSIGNED		
A3U19	1820 1202	7	1	IC GATE TTL LS NAND TPL 3 INP	01295	SN74LS10N
A3U20	1820 1281	2	1	IC DCDR TTL LS 2 TO 4 LINE DUAL 2 INP	01295	SN74LS139N

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U21	1820-1195	7	2	IC FF TTL LS D-TYPE POS EDGE TRIG COM	01295	SN74LS175N
A3U22	1820 1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U23	1820 1112	8		IC FF TTL LS D TYPE POS-EDGE TRIG	01295	SN74LS74AN
A3U24	1820 1208	3	3	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U25	1820 1196	8	8	IC FF TTL LS D TYPE POS EDGE TRIG COM	01295	SN74LS174N
A3U26	1820 1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U27	1820 1208	3		IC GATE TTL LS OR QUAD 2 INP	01295	SN74LS32N
A3U28	1820 1196	7		IC FF TTL LS D TYPE POS EDGE TRIG COM	01295	SN74LS175N
A3U29	1820 1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74AN
A3U30	1820 1203	8		IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A3U31	1820 0693	8	1	IC FF TTL S D TYPE POS EDGE TRIG	01295	SN74S74N
A3U32	1820 1196	6		IC FF TTL LS D TYPE POS EDGE TRIG COM	01295	SN74LS174N
A3U33	1820 1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74AN
A3U34	1820 1244	7	1	IC MUXR DATA SEL TTL LS 4 TO 1 L	01295	SN74LS153N
A3U35	1820 1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74AN
A3U36	1820 1144	6	2	IC GATE TTL LS NOR QUAD 2 INP	01295	SN74LS02N
A3U37	1820 1199	1		IC INV TTL TS HEX 1-INP	01295	SN74LS04N
A3U38	1820 1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U39	1820 1300	6	4	IC SHF RGTR TTL LS R S PRL IN PRL OUT	01295	SN74LS195AN
A3U40	1820 1300	6		IC SHF RGTR TTL LS R S PRL IN PRL OUT	01295	SN74LS195AN
A3U41	1820 1300	6		IC SHF RGTR TTL LS R S PRL IN PRL OUT	01295	SN74LS195AN
A3U42	1820 1300	6		IC SHF RGTR TTL LS R S PRL IN PRL OUT	01295	SN74LS195AN
A3U43	1820 1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74AN
A3U44	1820 1441	6	10	IC ADDR TTL LS BIN FUL ADDR 4 BIT	01295	SN74LS283N
A3U45	1820 1441	6		IC ADDR TTL LS BIN FULL ADDR 4 BIT	01295	SN74LS283N
A3U46	1820 1441	6		IC ADDR TTL LS BIN FULL ADDR 4 BIT	01295	SN74LS283N
A3U47	1820 1441	6		IC ADDR TTL LS BIN FULL ADDR 4 BIT	01295	SN74LS283N
A3U48	1820 1441	6		IC ADDR TTL LS BIN FULL ADDR 4 BIT	01295	SN74LS283N
A3U49	1820 1441	6		IC ADDR TTL LS BIN FULL ADDR 4 BIT	01295	SN74LS283N
A3U50	1820 1201	6		IC GATE TTL LS AND QUAD 2 INP	01295	SN74LS08N
A3U51	1820 1441	6		IC ADDR TTL LS BIN FULL ADDR 4 BIT	01295	SN74LS283N
A3U52	1820 1441	6		IC ADDR TTL LS BIN FULL ADDR 4 BIT	01295	SN74LS283N
A3U53	1820 1441	6		IC ADDR TTL LS BIN FULL ADDR 4 BIT	01295	SN74LS283N
A3U54	1820 1441	6		IC ADDR TTL LS BIN FULL ADDR 4 BIT	01295	SN74LS283N
A3U55	1820 1196	8		IC FF TTL LS D TYPE POS EDGE TRIG COM	01295	SN74LS174N
A3U56	1820 1444	9	2	IC MUXR DATA SEL TTL LS 2 TO 1 LINE QUAD	01295	SN74LS298N
A3U57	1820 1144	6		IC GATE TTL LS NOR QUAD 2 INP	01295	SN74LS02N
A3U58	1820 1204	9	1	IC GATE TTL LS NAND DUAL 4 INP	01295	SN74LS20N
A3U59	1820 1438	1	3	IC MUXR DATA SEL TTL LS 2 TO 1 LINE QUAD	01295	SN74LS257AN
A3U60	1820 1438	1		IC MUXR DATA SEL TTL LS 2 TO 1 LINE QUAD	01295	SN74LS257AN
A3U61	1820 1438	1		IC MUXR DATA SEL TTL LS 2 TO 1 LINE QUAD	01295	SN74LS257AN
A3U62	1820 1444	9		IC MUXR DATA SEL TTL LS 2 TO 1 LINE QUAD	01295	SN74LS298N
A3U63	1820 1196	8		IC FF TTL LS D TYPE POS EDGE TRIG COM	01295	SN74LS174N
A3U64	1820 1207	2	1	IC GATE TTL LS NAND 8 INP	01295	SN74LS30N
A3U65	1820 1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74AN
A3U66	1820 1307	3	1	IC SCHMITT TRIG TTL S NAND QUAD 2 INP	01295	SN74S132N
A3U67	1820 1196	7	1	IC FF TTL LS D TYPE POS EDGE TRIG COM	01295	SN74LS175N
A3U68	1820 1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74AN
A3U69	1820 1201	6		IC GATE TTL LS AND QUAD 2 INP	01295	SN74LS08N
A3U70	1820 1196	6		IC FF TTL LS D TYPE POS EDGE TRIG COM	01295	SN74LS174N
A3U71	1820 1196	8		IC FF TTL LS D TYPE POS EDGE TRIG COM	01295	SN74LS174N
A3U72	1820 1197	9		IC GATE TTL LS NAND QUAD 2 INP	01295	SN74LS00N
A3U73	1820 1416	5	1	IC SCHMITT TRIG TTL LS INV HEX 1 INP	01295	SN74LS14N
A3U74	1820 1074	1	2	IC DRVR TTL NOR QUAD 2 INP	01295	SN74128N
A3U75	1820 1074	1		IC DRVR TTL NOR QUAD 2 INP	01295	SN74128N
A3U76	1820 1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74AN
A3U77	1820 1423	4	2	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A3U78	1820 1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A3U79	1820 1203	8		IC GATE TTL LS AND TPL 3 INP	01295	SN74LS11N
A3U80	1820 1747	5	1	IC GATE CMOS NAND QUAD 2 INP	04713	MC14011BCP
A3U81	1820 1918	2	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
A3U82	1820 1348	2	1	IC GEN PMOS	27014	MM5307N
A3U83	1820 2204	1	1	IC UART CMOS	32293	IM6402 1IPL
A3U84	1820 0509	5	1	IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
A3U85	1820 0990	8	1	IC RCVR DTL NAND LINE QUAD	04713	MC1489AL
A3U86	1820 1199	1		IC INV TTL TS HEX 1-INP	01295	SN74LS04N
A3U87	1820 1112	8		IC FF TTL LS D TYPE POS EDGE TRIG	01295	SN74LS74AN
A3U88	1826 0282	3	1	IC V RGLTR TO 92	04713	MC79L12ACP
A3U89	1810 0076	0	2	NETWORK RES 9 SIP1 8K OHM - 8	28480	1810-0076
A3U90	1810 0076	0		NETWORK RES 9 SIP1 8K OHM - 8	28480	1810 0076
A3VR1	1902 3149	9	1	DIODE ZNR 9.09V 5% DO 35 PD 4W	28480	1902 3149
A3VR2	1902 3104	6	2	DIODE ZNR 5.62V 5% DO 35 PD 4W	28480	1902 3104
A3VR3	1902 3104	6		DIODE ZNR 5.62V 5% DO 35 PD 4W	28480	1902 3104
A3XE1	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP SLDR	28480	1200-0638
A3XE2	1200-0607	0	2	SOCKET-IC 16-CONT DIP DIP SLDR	28480	1200-0607
A3XE3	1200-0796	6	2	SOCKET-IC 8 CONT DIP DIP SLDR	28480	1200-0796
A3XE4	1200-0607	0	0	SOCKET IC 16-CONT DIP DIP SLDR	28480	1200-0607
A3XE5	1200-0796	6	2	SOCKET-IC 8-CONT DIP DIP SLDR	28480	1200-0796
A3XU83	1200 0654	7	1	SOCKET-IC 40-CONT DIP DIP SLDR	28480	1200 0654
A3Y1	0410 1004	7	1	CRYSTAL QUARTZ 1.8432 MHZ HC 33/U HLDR	28480	0410 1004

See introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
00000	ANY SATISFACTORY SUPPLIER			
00908	KEMET			
01121	ALLEN BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85062
18324	SIGNETICS CORP	SUNNYVALE	CA	94086
24546	CORNING GLASS WORKS (BRADFORD	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
32293	INTERSIL INC	CUPERTINO	CA	95014
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

This section normally contains information for adapting this manual to instruments for which the content does not apply directly. Since this manual does apply directly to instruments having the serial number listed on the title page, no change information is given here.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

This section contains schematics and theory of operation for the 1351A/001 Model 52105A RS-232 interface. These are to be used in conjunction with the HP-IB trouble-shooting procedure outlined in the 1351A Operating and Service manual.

Please refer to the 1351A Operating and Service manual for detailed explanations of the mnemonics and operation of the 1351A mainframe.

8-2. THEORY OF OPERATION.

A brief "get acquainted" description of 1351A operation is provided with the Simplified Block Diagram (figure 8-5) on page 8-5 of the 1351A Operation and Service Manual. Figure 8-3 contains samples of the schematic symbols.

8-3. LOGIC CONVENTIONS.

Positive logic convention is used in this manual, unless otherwise noted on the schematics. Positive logic convention defines a logic "1" as the more positive voltage (high) and a logic "0" as the more negative voltage (low).

8-4. MNEMONICS.

Signals in the 1351A/Option 001 have been assigned mnemonics that describe the active state and function of the signal line. A prefix letter (H, L, P, or N) indicates the active state of the signal. The remainder of the signal name indicates the function of the signal. An H prefix indicates the function is active in the high state; an L prefix indicates the function is active in the low state. For edge-controlled devices, the prefix P indicates the function is active on the positive-going transition; prefix N indicates the function is active on the negative-going transition.

8-5. LOGIC SYMBOLOGY.

This manual uses logic symbols as per American National Standards Institute standard Y32.14-1973. The purpose of these symbols is to graphically represent device functions so that operation can be understood without having to "look up" how a device works. Examples of ANSI Y32.14 symbols are provided in Figures 8-1 and 8-2.

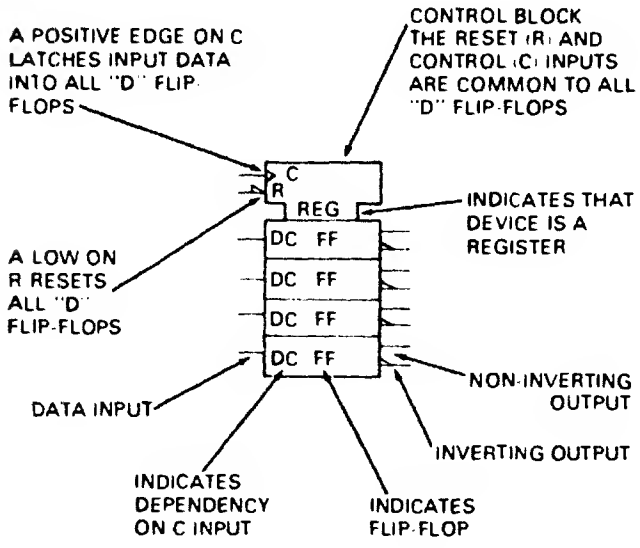


Figure 8-1. Symbol for a Quad D Flip-Flop

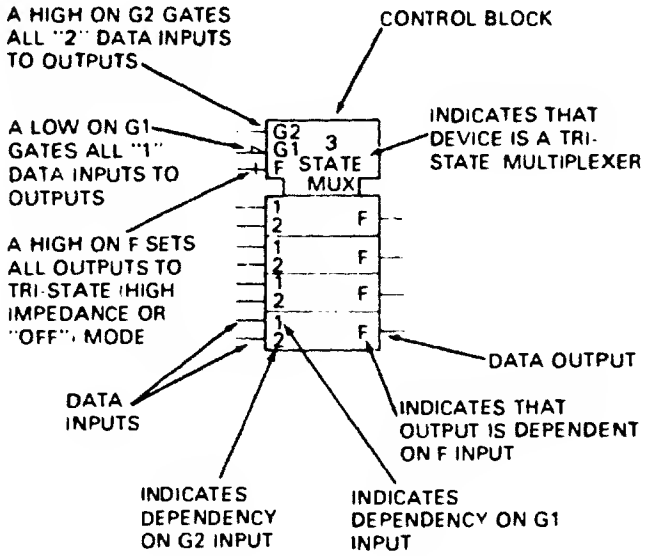


Figure 8-2. Symbol for a Quad Data Selector/Multiplexer

8-6. TROUBLESHOOTING.

WARNING

Maintenance and troubleshooting procedures described herein are performed with power applied to the instrument and protective covers removed. Service should be performed only by qualified personnel who are aware of hazards involved (such as fire or electrical shock). Read the Safety Summary at the front of this manual before troubleshooting the instrument.

8-7. TROUBLESHOOTING PROCEDURE.

Before troubleshooting in detail, try to perform the adjustment procedure in Section V of the 1351A Operating and Service Manual. Some apparent malfunctions may be corrected by these adjustments. Failure to obtain a correct adjustment may reveal the source of trouble.

If trouble is suspected, visually inspect the instrument. Look for loose or burned components that might suggest a source of trouble.

Verify that all circuit board connections are making good contact and are not shorting to an adjacent circuit. Sometimes a problem can be solved by cleaning printed circuit edge connectors with a non-abrasive pencil eraser and a clean cloth.

Check instrument power supply voltages and external power source.

The most important prerequisites for successful troubleshooting are: (a) an understanding of 1351A programming; and (b) a knowledge of 1351A circuit operation. An improper response to a programming command will often isolate the problem to a specific area.

8-8. TROUBLE DIAGNOSIS.

Since the 1351A/Option 001 is used in systems along with an X-Y display and a computer, any suspected fault should first be isolated to a specific instrument in the system. Suspected 1351A malfunctions may actually be malfunctions in the X-Y display or in the computer.

8-9. PREVENTIVE MAINTENANCE.

Cleaning. Painted surfaces can be cleaned with a commercial, spray-type window cleaner or with a mild soap and water solution.

CAUTION

Avoid using chemical cleaning agents that might damage the plastics used in this instrument. Recommended cleaning agents are isopropyl alcohol, kelite (1 part kelite, 20 parts water), or a solution of 1% mild detergent and 99% water.

Corroded spots are best removed with soap and water. Stubborn residues can be removed with a fine abrasive. Protect such areas from further corrosion with an application of silicone resin such as GE DRIFILM 88.

8-10. QUICK REFERENCE TO SERVICE SHEETS.

Table 8-1 is a reference to figures contained in the Service Sheets.

Table 8-1. Service Sheet Quick Reference

Figure No.	Title
8-4	I/O Board Simplified Block Diagram
8-5	I/O Board Component Locator
8-6	Schematic 2E (RS-232 Interface Circuitry)
8-7	Schematic 2A
8-10	Schematic 2B
8-11	Schematic 2C
8-12	Schematic 2D

8-11. GENERAL INFORMATION.

Input Output Assembly A3 contains the input connector for information from the RS-232 controller and output connectors for Display TTL blanking and Auxiliary control of a 1338A Tri-Color Display.

The Simplified Block Diagram (figure 8-4) for A3 shows major functional stages and their corresponding schematic locations. Detailed signal and stage descriptions are covered by the explanations of each of the five schematics.

Schematic 2A contains ASCII instruction decoding and handshake timing circuits. Schematic 2B contains control and timing circuits. Schematic 2C contains BCD to Binary converter and data output circuits. Schematic 2D contains auxiliary interface and power interrupt detection circuits. Schematic 2E contains RS-232 interface circuitry.

8-12. OPERATING OVERVIEW.

The 1351A Option 001 listens in one of two modes:

1) Program
2) Data

In the Listen For Program mode the 1351A receives two bytes from the RS-232 controller that define the 1351A instruction. These two-letter instructions are the Graphics Translator Machine Language (GTML) mnemonics.

After two program bytes are received, the 1351A Option 001 is placed into the Listen For Data mode. The 1351A Option 001 now receives parameter (or text) bytes until a ":" (colon), a CR (Carriage Return), or a LF (Line Feed) byte is received. The ":" (or CR or LF) causes the 1351A to return to the Listen For Program mode.

NOTE

If text is being received, an ETX (END OF TEXT) character must precede the ":" (or CR or LF).

Program Input Instruction Types.

All two-byte Program instructions are one of two types: (1) an Input Output board instruction; or (2) a Control Board instruction.

The four Input Output (I/O) Board instructions are:

1) Plot Absolute (PA)
2) Character Size (CS)

Data Types.

In the Listen For Data mode, all bytes received are either parameter bytes or text bytes.

Parameter bytes are converted to binary values on the I/O Board. Text bytes are not converted.

Data (parameter or text) is sent to the Control Board from the I/O Board via the ID1-ID13 lines.

ID1-ID13 Information Definition.

Information contained on ID1-ID13 is defines by: (a) type of instruction (I/O Board or Control Board); and (b) state of 1351A memory address line A0.

Three cases will be used to show ID1-ID13 information content for different instruction types. Each case is divided into two parts to show ID line definitions for A0 both low and high. The three cases are: (1) I/O Board instruction; (2) Control Board instruction other than Find Location (FLE and (3) Find Location Control Board instruction.

The 1351A memory capacity is 8192 words of 32 bits. Each 32-bit word contains two 16-bit bytes. Byte content is defined by the state of memory address line A0.

Refer to table 8-2.

CASE 1.

If an Input/Output Board instruction is detected, then ID1-ID10 are defined as follows.

a) When A0 = low:

1. If ID1-ID10 = 1023 (all high), then 1351A is in standard Text mode.

2. If ID1-ID10 = 1022 and CHAR ROM SELECT is high then 1351A is in alternate Text mode.

3. If ID1-ID10 < 1022, then 1351A is in Plot mode and ID1-ID10 is the binary X value.

b) When A0 = high:

1. If Text mode, then ID1-ID7 = ASCII character, ID8 and ID9 = character size (1,2,4,8), ID10 = rotate bit (low = 0; high = 90 degrees).

NOTE

CASE 2.

If a Control Board instruction other than Find Location (FL) is detected, then ID1-ID6 become PBO1-PBO6 and are defined as follows.

a) When A0 = low:

PBO1-PBO6 = file name (binary).

PBO1-PBO5 are for Erase File (EF), Name File (NF), Find File (FF), Blank File (BF), or Unblank File (UF) parameter.

b) When A0 = high:

PBO1 = Z-axis (Pen Enable command and parameter detected on I/O Board and sent separately to Control Board as Z-axis bit to become PBO1).

PBO2 = file blanking bit (used with BF and UF).

PBO3-PBO6 = TTL blanking bits (used with WX).

CASE 3.

If the Control Board instruction Find Location (FL) is detected, then ID1-ID13 = binary value (0-8191) used when A0 = low as the next write pointer to address 1351A memory.

Table 8-2. ID1-ID12 Definitions

A0 State	CASE 1. I/O Instruction (DO WRITE)	CASES 2&3. Control Board Instruction (Get Busy)
low	ID1-ID10 = 1023 or 1022 with CHAR SEL high is Text flag	Case 2. Not FL ID1-ID6 become PBO1-6 PBO1-PBO6 = file no.
	ID1-ID10 < 1022 is binary X value (Plot mode)	
		Case 3. FL instruction ID1-ID13 = binary X value used as next write pointer
high	If Text mode: ID1-ID7 = ASCII ID8&ID9 = character size ID10 = character rotation bit	Case 2. PBO1 = Z-axis bit PBO2 = file blanking bit PB03-PB06 = TTL blanking bits
	If Plot mode: ID1-ID10 = binary Y value	

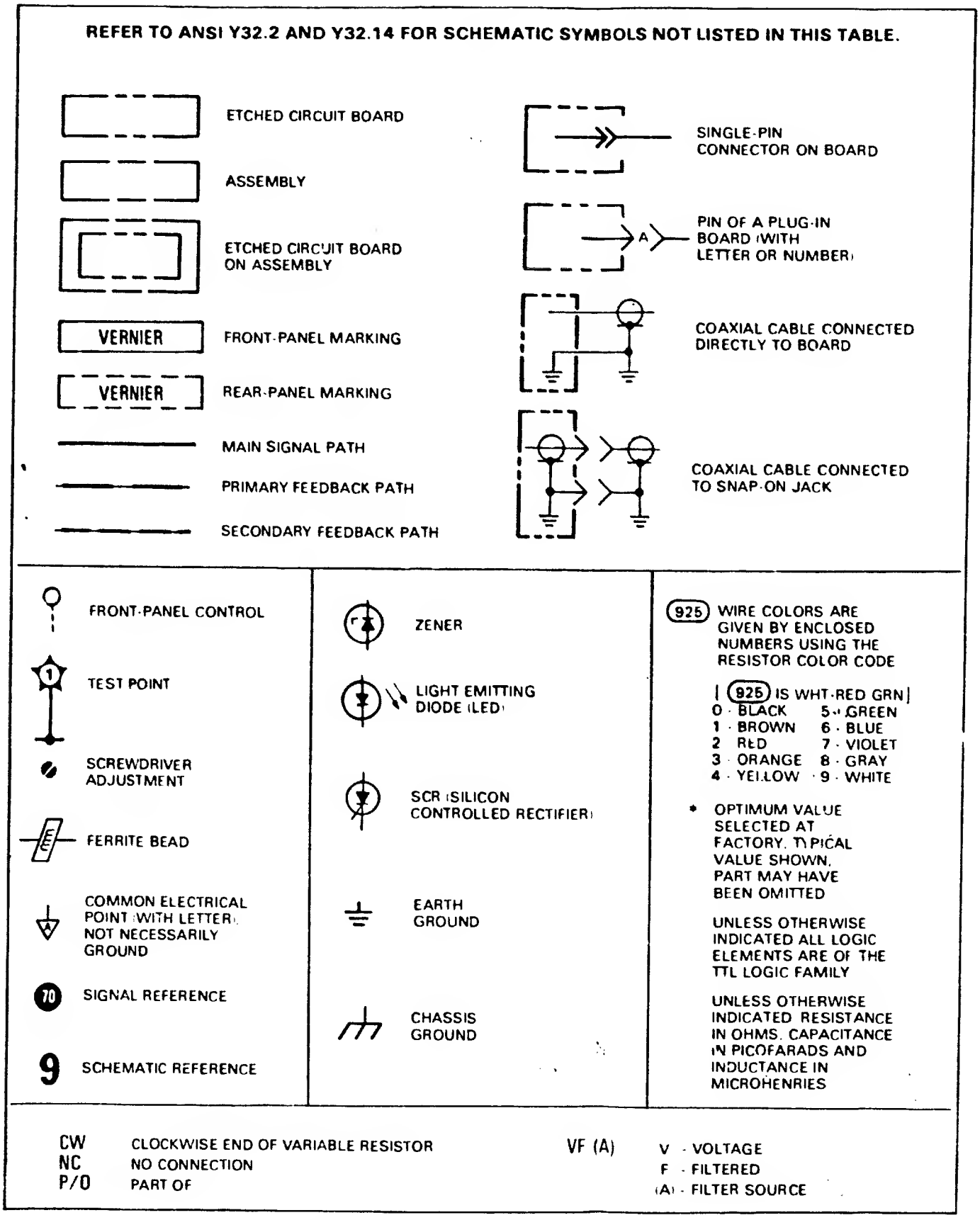


Figure 8-3. Schematic Diagram Symbols

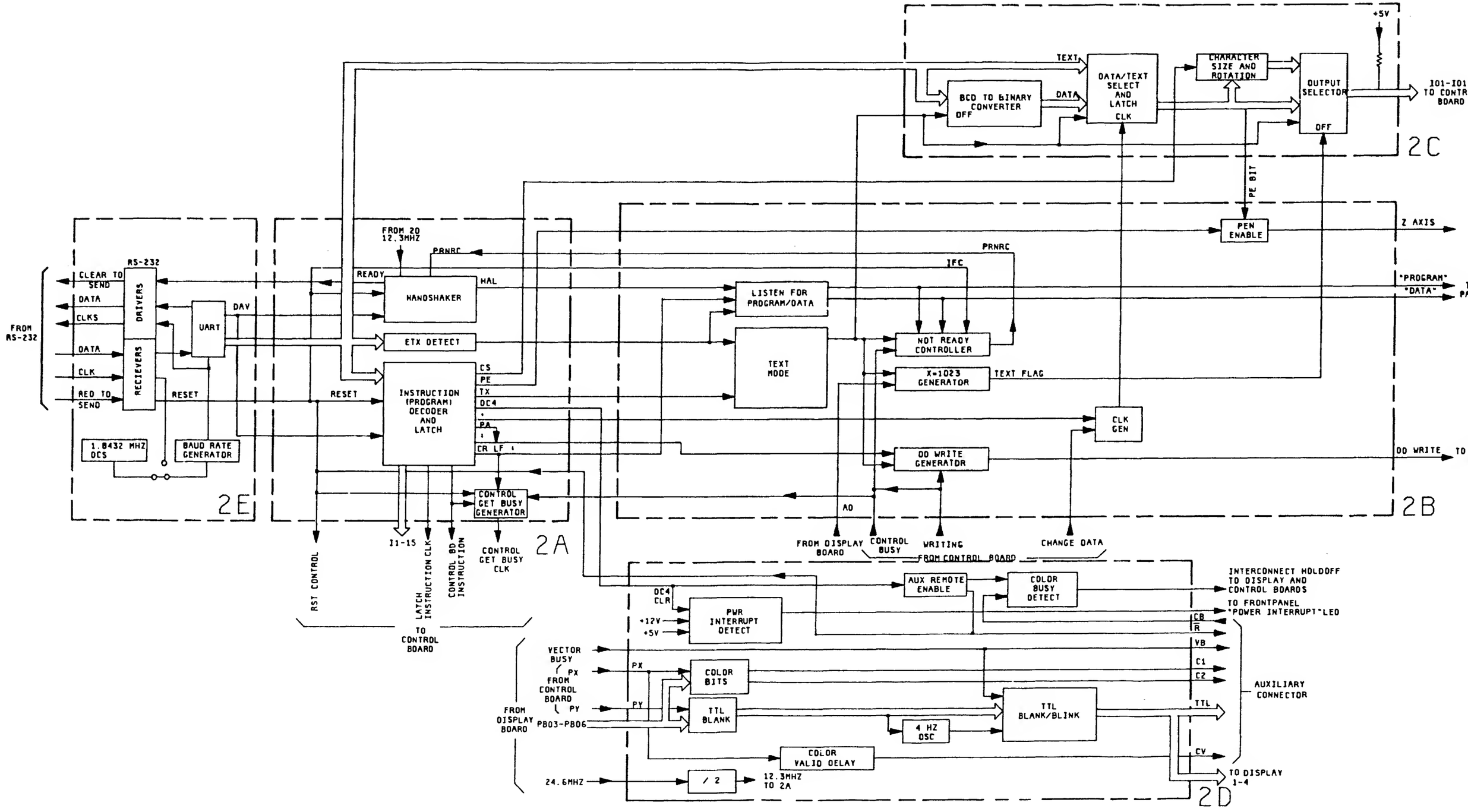


Figure
I/O Board A3 Simplified Block Diag

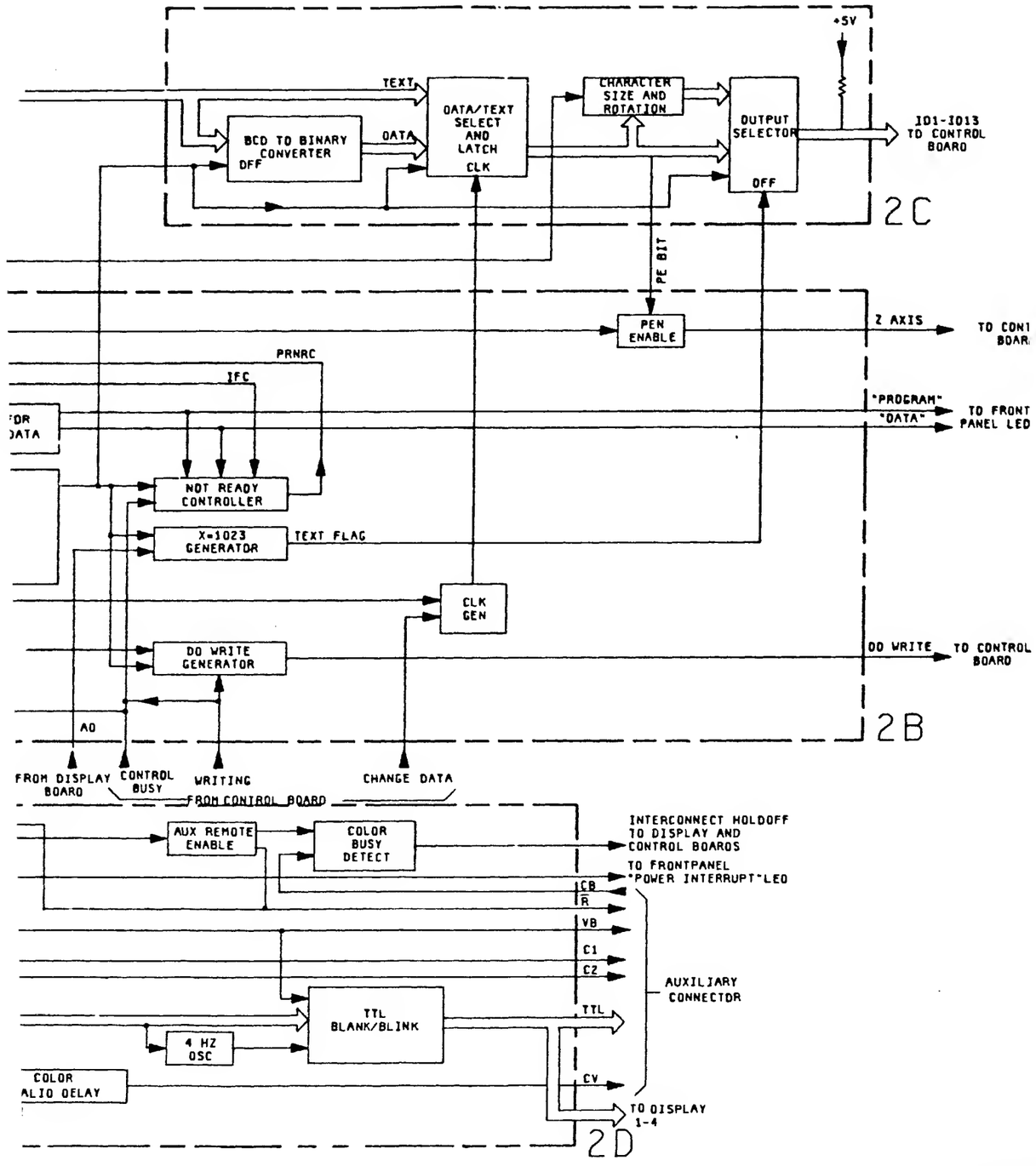


Figure 8-4
I/O Board A3 Simplified Block Diagram

8-13. SCHEMATIC 2E PRINCIPLES OF OPERATION.

The 2 Input/Output Assembly A3 allows the 1351A to receive serial data by first converting it into a parallel form the 1351A will understand.

Schematic 2E contains: (a) RS-232 to TTL, and TTL to RS-232 level translators/line receivers/drivers, (b) 1.8432 MHz oscillator, (c) switch programmable divider for baud-rate selection, (d) UART for serial data I/O, (e) RS-232 handshake lines, (f) clock gating, (g) internal bus buffers, and (h) Time-Out Reset circuitry.

8-14. LEVEL TRANSLATORS/LINE DRIVERS/LINE RECEIVERS.

U84 is a TTL to RS-232 level translator and line driver. U84A is used to drive H=Serial Data Out. S1-2 is normally open; serial data is generally not transmitted from the 1351A. U84B is used to output RS-232 Level Clock. U84D is used to output H=Clear To Send.

U85 is an RS-232 to TTL level translator and line receiver. U85A is used to receive an external clock signal. U85B receives Serial Data In. U85D receives Request To Send.

8-15. PROGRAMMABLE DIVIDER.

Sections 5-8 of switch S2 (pins 8-11 of U82), allow the to select a number of different baud rates when using external clock or internal oscillator. The following table is frequency output as a function of switch settings.

Table 8-3. Baud Rate Selection

U82 Pin 5 6 7 8	Output Freq	Baud Rate (Output Freq ÷ 16)
0 0 0 0		Ext. Freq.
0 0 0 1	800	50
0 0 1 0	1200	75
0 0 1 1	1760	110
0 1 0 0	2152	134.5
0 1 0 1	2400	150
0 1 1 0	4800	300
0 1 1 1	9600	600
1 0 0 0	14,400	900
1 0 0 1	19,200	1200
1 0 1 0	28,800	1800
1 0 1 1	38,400	2400
1 1 0 0	57,600	3600
1 1 0 1	76,800	4800
1 1 1 0	115,200	7200
1 1 1 1	153,600	9600

8-16. UART (UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER).

UART U83 serves as the controller for receiving functions of the interface. The receiver portion converts serial data to parallel data. Start, stop, parity, overrun, and framing errors are ignored by the 1351A/Option 001. Parallel data (7 bits) output is on pins 6-12. This 7-bit format is right-justified to RD1. When using 8-bit serial input format, the corresponding output (parallel) will be 7 bits wide with the most significant (RD8) truncated.

Data on pin 20 (H=Serial Data In) is clocked in by the H=Trans/Rcv Clock on pin 17. This clock is 16 times the data rate.

Pin 21 is the UART H=Reset. A high level does not clear the receiver buffer register, but is required after power up. Approximately 18 clocks after H=Reset goes low, L=Talk (pin 24) goes high.

H Serial Data Out from the UART (pin 25) is gated through U84A.

Pin 34 of the UART is tied high so the control signals at pins 35, 36, 38, 39 are continuously loaded into the internal control register. The control signals loaded into this register determines character length (7 or 8 bits), stop bit select (1 or 2 bits), parity enable, and parity type (even or odd).

These control inputs are switch selectable by sections 1-4 of switch S2. The functions are described in table 8-4.

Table 8-4. UART Control Word Functions

U83 Pin 35	36	38	39	Parity	No. of Stop Bits
L	L	L	L	Odd	1
L	L	L	H	Even	1
L	H	L	L	Odd	2
L	H	L	H	Even	2
H	L	L	X	Disabled	1
H	H	L	X	Disabled	2

L = 0
H = 1
X = Don't Care

8-17. RS-232 HANDSHAKE LINES.

U16A pin 1 is held high through CR4 (except during a time-out reset). H=Ready is gated through U16A (now H=Interface Busy) and inverted by U84D. This becomes H=Clear To Send and holds off any data transfer until the current data or instruction has been processed.

L=Interface Reset is an external reset through U85D (H=Request To Send) that accomplishes a reset by pulling the L=Interface Reset line low through CR4. The status of H=Interface Busy remains unchanged.

8-18. CLOCK GATING.

Both the RS-232 and TTL level clocks are gated only when H=Ready is true and is used with computers not having a seperate RS-232 clock on the transmission card. Such a configuration eliminates the need to transmit an H=Clear To Send command to the host computer.

8-19. INTERNAL BUS BUFFERS.

U81 provides non-inverted (H=DIO1-7) drive for the instruction decoder (schematic 2A) and the BCD to Binary converter (2D). U86 provides inverted (L=DIO3-7) drive for the End Of Text decoder (2B).

8-20. U57D TIME-OUT RESET.

Should H=READY remain low for more than approximately 2.5 seconds, the time-out circuit resets the interface. This keeps the 1351A from "hanging up" in case it receives a command it cannot execute, such as FF (Find File) when no such file exists. When the base of Q5 is low, Q5 will not conduct and C55 charges through R62. When C55 reaches the trigger voltage of unijunction Q6, Q6 will "fire" and a positive pulse is seen through U57D. U57D inverts the pulse and causes CR5 to forward bias. L=IFC pulls low through CR6 and clears U23A (schematic 2B). It also clocks Ready Latch to signal the controller H=Clear To Send.

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG
C2	F-5	C39	J-6	L1	M-1	R28	M-8	R68	8-5	U33
C4	H-6	C40	E-6	Q1	M-6	R29	L-7	R69	8-5	U34
C5	C-6	C41	E-7	Q2	M-6	R30	K-7	R70	D-3	U35
C6	N-3	C42	H-7	Q3	N-6	R31	K-7	R71	L-6	U36
C7	M-5	C43	L-8	Q4	N-6	R32	M-7	R72	L-6	U37
C8	G-3	C44	J-8	Q5	N-5	R33	D-7	R73	D-5	U38
C9	N-5	C45	F-3	Q6	N-5	R34	D-7	R74	D-5	U39
C10	D-5	C46	F-6	Q7	L-5	R35	8-7	R75	C-4	U40
C11	L-7	C50	D-4	R2	E-1	R36	L-7	S1	C-5	U41
C12	K-7	C51	D-4	R3	E-1	R37	N-6	S2	C-4	U42
C13	D-7	C52	C-4	R4	D-1	R38	J-8	S3	K-8	U43
C14	D-7	C53	D-3	R5	C-1	R39	J-8	U1	C-6	U44
C15	8-7	C54	D-4	R6	F-5	R40	J-8	U7	C-1	U45
C16	8-8	C55	M-5	R7	F-5	R41	J-8	U8	D-6	U46
C17	C-6	C56	L-7	R8	H-7	R42	8-8	U9	D-5	U47
C18	8-7	C57	N-5	R9	H-7	R43	8-8	U10	D-4	U48
C19	8-5	C58	D-4	R10	C-6	R44	8-7	U14	D-1	U49
C20	8-7	C59	N-4	R11	C-6	R45	8-7	U15	E-6	U50
C21	N-2	C60	N-4	R12	G-1	R46	8-5	U16	E-5	U51
C22	E-7	C61	F-8	R13	G-1	R47	8-5	U17	E-4	U52
C23	C-2	C62	E-8	R14	M-6	R48	8-5	U19	E-3	U53
C24	E-2	CR1	K-7	R15	N-6	R49	8-5	U20	E-2	U54
C25	F-2	CR2	8-7	R16	M-6	R50	M-7	U21	E-1	U55
C26	G-1	CR3	8-5	R17	M-6	R53	F-3	U22	F-6	U56
C27	K-1	CR4	8-5	R18	M-5	R54	F-7	U23	F-5	U57
C28	L-1	CR5	8-5	R19	M-5	R55	F-7	U24	F-4	U58
C29	K-3	CR6	8-5	R20	G-2	R60	N-6	U25	F-4	U59
C30	F-3	E16	8-3	R21	G-3	R61	M-5	U26	F-3	U60
C31	G-4	E34	G-7	R22	M-7	R62	N-5	U27	F-2	U61
C32	C-5	E35	G-7	R23	M-7	R63	N-5	U28	F-1	U62
C33	F-4	E36	M-7	R24	M-7	R64	N-5	U29	G-6	U63
C34	D-4	E37	M-7	R25	M-7	R65	L-7	U30	G-5	U64
C36	E-5	E38	E-3	R26	M-8	R66	M-5	U31	G-4	U65
C37	K-5	J1	A-3	R27	M-8	R67	L-7	U32	G-4	U66
C38	K-6	J2	A-6							

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C2	F-5	C39	J-6	L1	M-1	R28	M-8	R68	B-5	U33	G-3	U67	K 8
C4	H-6	C40	E-6	Q1	M-6	R29	L-7	R69	B-5	U34	G-2	U68	J-7
C5	C-6	C41	E-7	Q2	M-6	R30	K-7	R70	D-3	U35	G-1	U69	H-8
C6	N-3	C42	H-7	Q3	N-6	R31	K-7	R71	L-6	U36	H-6	U70	H-7
C7	M-5	C43	L-8	Q4	N-6	R32	M-7	R72	L-6	U37	H-5	U71	G-8
C8	G-3	C44	J-8	Q5	N-5	R33	D-7	R73	D-5	U38	H-4	U72	G-7
C9	N-5	C45	F-3	Q6	N-5	R34	D-7	R74	D-5	U39	H-4	U73	F-8
C10	D-5	C46	F-6	Q7	L-5	R35	8-7	R75	C-4	U40	H-3	U74	E-8
C11	L-7	C50	D-4	R2	E-1	R36	L-7	S1	C-5	U41	H-2	U75	E-7
C12	K-7	C51	D-4	R3	E-1	R37	N-6	S2	C-4	U42	H-1	U76	D-8
C13	D-7	C52	C-4	R4	D-1	R38	J-8	S3	K-8	U43	J-6	U77	C-8
C14	D 7	C53	D-3	R5	C-1	R39	J-8	U1	C-6	U44	J-5	U78	C-7
C15	B-7	C54	D-4	R6	F-5	R40	J-8	U7	C-1	U45	J-4	U79	F-7
C16	B-8	C55	M-5	R7	F-5	R41	J-8	U8	D-6	U46	J-4	U80	L-7
C17	C-6	C56	L-7	R8	H-7	R42	B-8	U9	D-5	U47	J-3	U81	D-3
C18	B-7	C57	N-5	R9	H-7	R43	B-8	U10	D-4	U48	J-2	U82	C-4
C19	B-5	C58	D-4	R10	C-6	R44	B-7	U14	D-1	U49	J-1	U83	C-2
C20	B 7	C59	N-4	R11	C-6	R45	B-7	U15	E-6	U50	K-6	U84	E-4
C21	N-2	C60	N-4	R12	G-1	R46	B-5	U16	E-5	U61	K-5	U85	D-4
C22	E 7	C61	F-8	R13	G-1	R47	B-5	U17	E-4	U52	K-4	U86	C-3
C23	C-2	C62	E-8	R14	M 6	R48	B-5	U19	E-3	U53	K-4	U87	J 7
C24	E-2	CR1	K 7	R15	N-6	R49	B-5	U20	E-2	U54	K-3	U88	D-4
C25	F-2	CR2	B 7	R16	M-6	R50	M 7	U21	E-1	U55	K-2	U89	M-4
C26	G-1	CR3	B-5	R17	M-6	R53	F-3	U22	F-6	U56	K-1	U90	M-4
C27	K-1	CR4	B-5	R18	M 5	R54	F-7	U23	F-5	U57	L-6	VR1	L-7
C28	L-1	CR5	B-5	R19	M-5	R55	F 7	U24	F-4	U58	L-5	VR2	G 3
C29	K-3	CR6	B 5	R20	G-2	R60	N-6	U25	F-4	U59	L-4	VR3	G-3
C30	F-3	E16	B-3	R21	G-3	R61	M-5	U26	F-3	U60	L-4	XE1	B-5
C31	G-4	E34	G-7	R22	M 7	R62	N-5	U27	F-2	U61	L-3	XE2	B-4
C32	C-5	E35	G-7	R23	M-7	R63	N 5	U28	F-1	U62	L-2	XE3	B 3
C33	F-4	E36	M-7	R24	M 7	R64	N-5	U29	G-6	U63	L-1	XE4	B-7
C34	D-4	E37	M-7	R25	M 7	R65	L-7	U30	G-5	U64	B-1	XE5	N-1
C36	E 5	E38	E-3	R26	M-8	R66	M 5	U31	G-4	U65	L-8	XEB3	C-2
C37	K-5	J1	A 3	R27	M 8	R67	L-7	U32	G-4	U66	L-7	Y1	N-7
C38	K-6	J2	A-6										

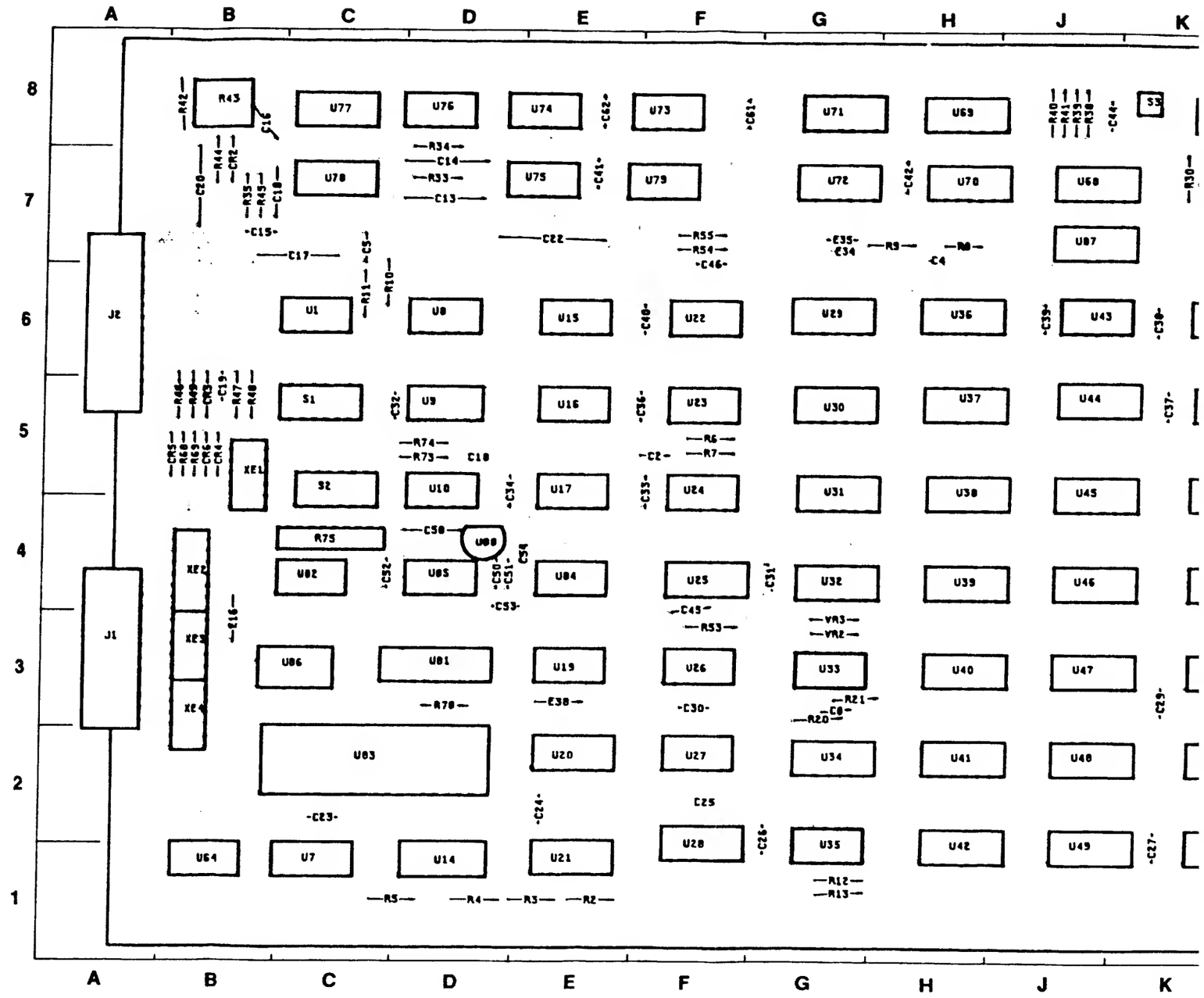
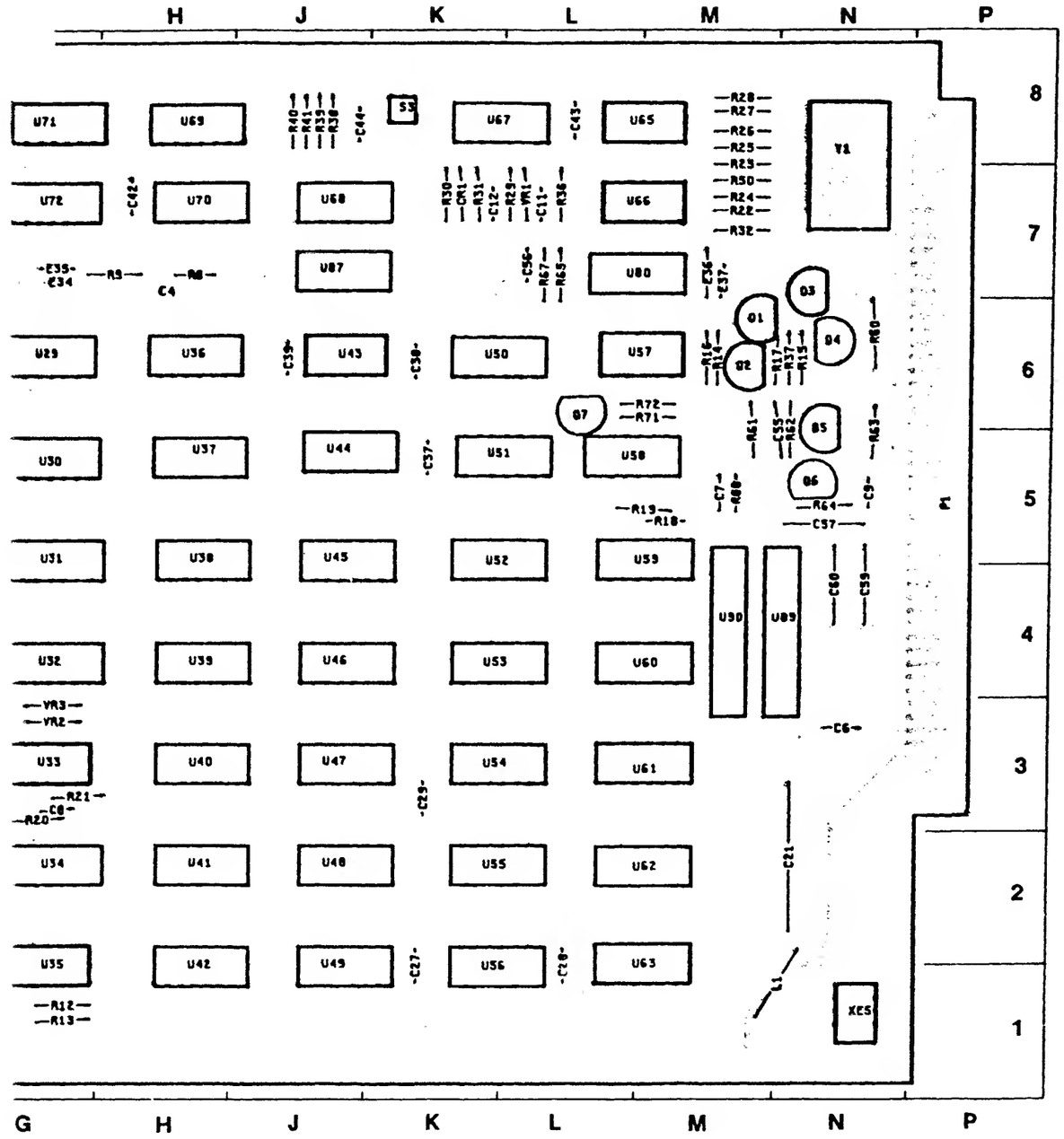


Figure 8-5. I/O Board A3 Component Locator



Component Locator

P/O A3 RS-232 I/O (52105-6650I)

U84,85 RS232C/TTL LEVEL TRANSLATORS

+15V -15V E1 E4 E3 E2

S1-3 SERIAL DATA IN 4 U85B 6 C50 430

E24 E23 SERIAL DATA OUT 3 U84A 2 S1-2

E21 E22 13 U85D 11 C51 430 U10B 3 4 INTERFACE RESET

E20 E19 E7 11 U84D 12 13 +5V 3 U16A 1 2 INTERFACE BUSY

E6 E16 10K E15 E31 E5 E13 E14

VR2 5.62V -15V C53 0.01 UF U84-(1)

VR3 5.62V +15V C54 0.01 UF U84-(14)

E18 E17 E8 6 U84B 4 5 RS-232 CLOCK

E10 E9

E12 E11 X16 CLOCK IN 1 U85A 3 +5V C52 430 2 R60 47 E32

S1-1 TTL CLOCK

E27 +15V E30

E25 -15V E26

E29 +5V E28

E39

Q4

E36 2000 E37 300 E35 E34 X 8 CLOCK

X 16 CLOCK U16D 11 12 13

U80A 1 2 3 R67 909K U80B 5 6 4

R65 220 Y1 1.8432 MHZ C56 10

U80,87 INTERNAL OSCILLATOR

U87A 2 3 4 1 5 6

U76A 2 3 4 1 5 6 NC

P/O R75 1000 +5V

P/O S2

E33 EXT FREQ CLK A B C D OUT RESET U82 3 13 4 7 +5V 12V

PROGRAMMABLE DIVIDER

L=RESET FROM U10 (8) 64 2A

UART +5V U83

P/O R75 ALL 1000

P/O S2

TO1 TO2 TO3 TO4 TO5 TO6 TO7 TO8

NC

R70 1000

U81 H=DI07 H=DI06 H=DI05 H=DI04 H=DI03 H=DI02 H=DI01 60 2A

H=DAV TO U10(1),U25(1,3),U15(3) 61 2A

U86 L=DI03 L=DI04 L=DI05 L=DI06 L=DI07 60 2A

KEYBOARD CONNECTION J3

H K J H G F E D B A C

(11) (10) (9) (8) (7) (6) (5) (4) (2) (1) (3)

TD8 TD7 TD6 TD5 TD4 TD3 TD2 TD1 TRANS CHAR E38 +5

U37E 11 10 R71 47K Q7 R72 180 L=TALK P/O P1 55

P/O XA3P1 6B P/O A2 INTER CONNECT ASSY

H=RESET L=DAC FROM U10(6) 65 2A

FROM U87(9) 62 2A

H=READY FROM U43(8) 66 2A

TIME OUT

RESET

R62 150K R63 1000 Q6 C55 22UF R61 10K Q5 C57 1000 R64 180 R66 180

U57D 12 13 11

CR4 CR5 CR6 R68 1000 R69 10K +5V -15V

L=INTERFACE RESET TO U9(2) 63 2A

U86F 12 13

-12V REGULATOR

U86 C I O -15V C59 15UF -12V C58 2.2UF

POWE

+5V 14 7 U10,1 57,76

NOTES

1. GATES / FUNCTI

2. UNLESS RESIS CAPAC INDUC

3. UNLESS LOGIC +2. 0V

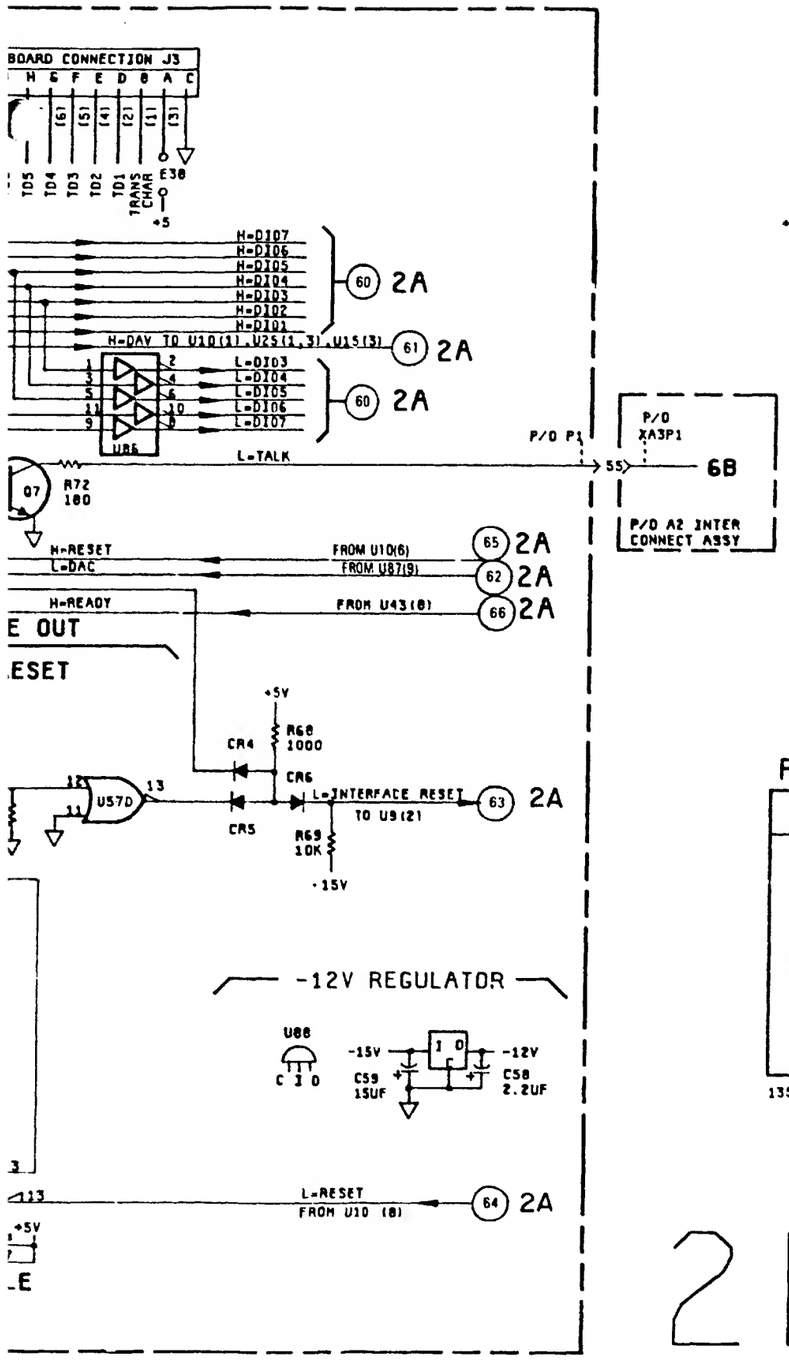
4. E1-3

PARTS O

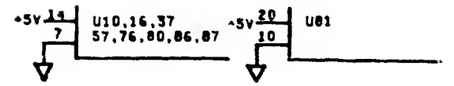
C50-59
CR4-6
J1,3
E1-39
Q4-7
R60-72,75
U10B,16A8,37E,
U81-83,84ABD,8
VR2,3
Y1

1351/RS232/600

2E



IC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC "1"=H
   0V TO +0.8V=LOGIC "0"=L
4. E1-39 SHOWN AS CONFIGURED BY FACTORY

PARTS ON THIS SCHEMATIC

P/O A3

C50-59
CR4-6
J1,3
E1-39
Q4-7
R60-72,75
U10B,16AB,37E,57D,76A,80AB,
U81-83,84ABD,85ABD,86,87A,88
VR2,3
Y1

1351/RS232/600

2E

Figure 8-6.
Schematic 2E
8-7

8-21. SCHEMATIC 2A PRINCIPLES OF OPERATION.

Schematic 2A contains: (a) Reset; (b) Handshake circuits; (c) Instruction Decode and Latch; and (d) Control Get Busy control.

8-22. RESET.

After the 1351A is powered on (or whenever a new program is sent to the 1351A) the Controller sets its H=Request To Send momentarily high. This RS-232 signal becomes the I/O Board's L=Reset.

L=Reset clears Control Get Busy Latch (U23A), Listen For Program Latch (2B-U1A) and Text Mode Latch (2B-U29A). L=Reset also clocks Ready Latch (U43A via 2B-U16B). Ready Latch signals H=Clear To Send and enables the clock gate (schematic 2E).

8-23. DATA MODE.

Once reset, the 1351A will receive its device dependent commands (GTML mnemonics) and required parameters.

First the 1351A goes to Listen For Program mode. Two bytes are received, decoded by Instruction Decoder U7, and latched into Instruction Latch U28 and U21.

After two Program bytes, the Listen For Program Latch (2B-U1A) is clocked to Listen For Data. Parameter (or text) bytes are received until a ":" (colon), CR (Carriage Return) or a LF (Line Feed) byte is received. When this happens the Latch returns to Listen For Program.

CR, LF, and ":" bytes are detected by U14 and U21B. Since U14 is disabled in Text mode, the 1351A must receive an ETX (End of Text) byte before it will be able to exit Text mode and return to Listen For Program. ETX is detected by U64.

Handshake Precision Timing Generator.

After each byte is received from RS-232, whether instruction "program" or data, Read Latch U43 must be clocked by P=RNRC (Release Not Ready Condition). This allows the 1351A to signal RS-232 Clear To Send, gate the Transmit/Receive clock (if so configured) and receive the next serial byte.

Approximately 250 ns after H=DAV goes high, U25 causes U43B to be clocked so that U32 is released to count. U32 produces clock signals for schematic 2B that control latching of DIO parameter (or text) bytes on schematic 2C.

Approximately 500 ns after H=DAV goes high, L=DAC is set low by U25. L=DAC returns high as soon as H=DAV is returned low by UART (2E-U83) indicating receive buffer empty.

Ready Latch U43 must now be clocked by P=RNRC in order for the next serial byte to be sent.

Control Board Instructions.

Program instructions are either I/O Board or Control Board instructions. When a Control Board two-byte instruction is detected, CTRL INST goes low. The negative edge of this level change is passed by C2 so that U23A sees a momentary low pulse on its set input. When set, U23A enables U36A.

When a ":" (or CR or LF) delimiter is detected, U19C produces a positive edge that latches the instruction (I1-I5) on the Control Board.

The ":" (or CR or LF) also allows U36A to enable U58C. Approximately 570 ns after the instruction latch clock (U19C), a negative edge is produced by U58C that tells the Control Board to act on the command (Control Get Busy).

After sensing a Control Get Busy clock, the Control Board signals its "busy" status by setting CTRL BUSY low. When the Control Board has finished processing the command it returns CTRL BUSY high. This positive edge clocks U23A inverting output high. U36A and U58C are now disabled until the next Control Board instruction is detected.

The positive edge of CTRL BUSY also causes a P=RNRC clock to be produced (schematic 2B) so that the 1351A can signal Ready For Data.

If the Control Board never returns CTRL BUSY high, then P=RNRC will not set Ready Latch. The 1351A will "hang up" until a Time Out Reset (schematic 2E) is produced upon the system L=Reset line. This time out is approximately 2.5 seconds. This can occur when a file is addressed via FF, EF, BF, or UF that was not previously named (NF#).

I/O Board Instructions.
When an Input/Output Board "program" instruction is detected CTRL INST goes high. Latch Instruction clock and Control Get Busy clock are inhibited.

I/O instruction Decoder U20 controls signals to I/O Board circuits on schematics 2B and 2C. I/O Board "program" instructions are: (1) Pen Enable (PE); (2) Character Size (CS); (3) Text (TX); and (4) Plot Absolute (PA).

Table 8-5. A3 U7 ROM (1816-1120) Character Decoding

DIO Address Lines 7	6	5	4	3	2	1	Decimal Value	Char. ASCII	U7 Output Pins MSB 9	10	11	LSB 12
0	0	0	0	0	1	1	3	ETX	0	0	0	1
0	0	0	1	0	1	0	10	LF	0	1	1	0
0	0	0	1	1	0	1	13	CR	0	1	1	0
0	0	1	0	1	0	0	20	DC4	0	1	0	1
0	1	0	1	1	0	0	44	,	0	1	0	0
0	1	1	1	0	1	0	58	:	0	1	1	0
0	1	1	1	0	1	1	59	;	0	0	1	1
1	0	0	0	0	0	1	65	A	0	1	1	1
1	0	0	0	0	1	0	66	B	1	1	0	0
1	0	0	0	0	1	1	67	C	0	0	0	0
1	0	0	0	1	0	1	69	E	1	0	0	0
1	0	0	0	1	1	0	70	F	1	1	1	0
1	0	0	1	1	0	0	76	L	1	0	0	0
1	0	0	1	1	0	1	77	M	0	1	0	0
1	0	0	1	1	1	0	78	N	1	0	0	1
1	0	1	0	0	0	0	80	P	0	0	1	1
1	0	1	0	0	1	1	83	S	1	0	1	0
1	0	1	0	1	0	0	84	T	0	0	1	0
1	0	1	0	1	0	1	85	U	1	0	1	1
1	0	1	0	1	1	1	87	W	1	1	0	1
1	0	1	1	0	0	0	88	X	0	0	0	0
1	1	0	0	0	0	1	97	a	0	1	1	1
1	1	0	0	0	1	0	98	b	1	1	0	0
1	1	0	0	0	1	1	99	c	0	0	0	0
1	1	0	0	1	0	1	101	e	1	0	0	0
1	1	0	0	1	1	0	102	f	1	1	1	0
1	1	0	1	1	0	0	108	l	1	0	0	0
1	1	0	1	1	0	1	109	m	0	1	0	0
1	1	0	1	1	1	0	110	n	1	0	0	1
1	1	1	0	0	0	0	112	p	0	0	1	1
1	1	1	0	0	1	1	115	s	1	0	1	0
1	1	1	0	1	0	0	116	t	0	0	1	0
1	1	1	0	1	0	1	117	u	1	0	1	1
1	1	1	0	1	1	1	119	w	1	1	0	1
1	1	1	1	0	0	0	120	x	0	0	0	0

Note: 0 = low; 1 = high.

P/O A3 INPUT/OUTPUT ASSY RS-232 52105-665011

2E (60) H=DI01-7 L=DI03-7

ETX DETECTOR

H=DI01
H=DI02
L=DI03
L=DI04
L=DI05
L=DI06
L=DI07

U64

NC

U15 B

H=TEXT MODE

FROM U16 (6) 2B (2)

+5V

READY LATCH

PRMRC

U43A FF

U43B FF

NC

L=READY

H=READY

L=EXT

FROM U31 (5) 2D (1) CLK 1

U32 REG

DC FF

HANDSHAKE PRE
GENER

L=RETU
L=E
P=2
P=1

2E (61) U61 (3) H=DAV

U10 A

L=DAV

H=DI01
H=DI02
H=DI03
H=DI04
H=DI05
H=DI06
H=DI07

U7

X=Y

A=255

ROM

AG 0
AG 1
AG 2
AG 3

R2 470
R3 470
R4 470
R5 470

INSTRUCTION DECODER

+5V

U14 OG X=Y

1G 2G 3G 4G 5G 6G 7G

NC

(,) COMMA
(;) SEMICOLON
(DC4) 20 10

DETECTOR

U24 B

INSTRUCTION LATCH

1ST PROGRAM BYTE=U28
2ND PROGRAM BYTE=U21

U28 REG

U21 REG

I3 I4 I5 I1 I2

I/O BD INSTRUC DECODER (PE,CS,TX,PA)

U79 C

+5V 12 U87 FF 8 NC 9 L=DAC U83(18) (62) 2E

2E (63) CR6

+5V

R73 2700

2D (59) C10 U76(8) .01UF

R74 2200

U9A

U10 C

U10 D

(64) U82(13) 2E

(65) U83(21) 2E

L=RESET

ETX DETECTOR

READY LATCH

HANDSHAKE PRECISION TIMING GENERATOR

INSTRUCTION DECODER

DETECTOR

INSTRUCTION LATCH

I/O BD INSTRUCTION DECODER

LOGIC DEVICE POWER CONNECTIONS

+5V 16 8 — U7,12,14 U20,21,25,28 U32

+5V 14 7 — U9,10,13,15,16 U23,24,36, U43,58,64,79

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCU FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC "1"=H
   0V TO +0.8V=LOGIC "0"=L

PARTS ON THIS SCHEMATIC

P/OA2 INTERCONNECT

P/O A3

C2,10,45
P/O P1
R2-7,53,73,74
U7,9AC,10ACE,U12-14,15AB,16C
U19AC,U20,21,23A,24BC,U25,
U28,32,36A,43,58B,64,79C

1351A/129/RS232/8/26/81

2A

Figure 8-7.
Schematic 2A
8-9

8-24. SCHEMATIC 2B PRINCIPLES OF OPERATION.

Schematic 2B is made up of circuits that: (a) determine whether the 1351A is in "listen for program" or "listen for data"; (b) indicate when the 1351A can signal that it is ready for the next byte from RS-232; (c) produce the DO WRITE signal; and (d) provide Pen Enable (Z-axis) status to the Control Board.

8-25. LISTEN FOR PROGRAM/DATA CIRCUITS.

Listen for Program.

After the 1351A/Option 001 receives a Request To Send, U1B and U79A/B are enabled. Ready For Program Byte Latch U17A controls the handshaking of "program" bytes from RS-232 by producing P = RNRC (via U58A and U16B) to release the Not Ready condition on schematic 2A. U79A and U79B produce clock edges that latch the two instruction "program" bytes on schematic 2A.

When Listen For Program/Data Latch U1A is first set to Listen For Program mode, the negative-going edge from U37D output is passed by C5. This sets Data Enable After Program Controller U8B, preventing the Ready For Data Byte sequence from occurring until after the 1351A has gone to Listen For Data.

Listen For Data.

When the second "program" byte is received, U1B inverting output (in the Instruction Latch Clock Generator) produces a positive edge. This clocks U1A, U29A, and U8B.

Listen For Program/Data Latch U1A (Q = high), turns Q2 on and Q1 off. LDATAL (Low, Data Listen) goes low to turn on front-panel "LISTEN FOR DATA" LED. LPROGL goes high to turn off front-panel "LISTEN FOR PROGRAM" LED. U37F disables the Instruction Latch Clock Generator while in Listen For Data.

Text Mode Latch U29A reports whether or not a Text (TX) instruction was received.

Data Enable after Program Controller U8B now permits the Ready for Data Byte sequence if not in Text mode. This sequence allows the 1351A to capture parameter bytes from RS-232 until the 1351A receives a ":" (or CR or LF). Ready For Data Byte Latch U8A Q output gets clocked high when a parameter byte is received from RS-232. This turns on 12.3 MHz CLK2 for four pulses (schematic 2D). Four State Counter U33A/B causes DIO1-DIO4 to be converted from parallel to serial and stored (schematic 2C). After the fourth state, U33B causes U8A to be reset (via U30C) and the 1351A can signal that it is ready for the next data byte from RS-232.

The parameter binary value is latched for output to the Control Board by a "," (comma) from RS-232. This negative clock edge is produced by Data/Text Selector and Latch Clock Generator U57A.

If Text Mode Latch U29A indicates that a Text (TX) instruction has been received, then text byte handshaking from RS-232 is controlled by Ready For Text Byte Latch U29B.

8-26. DO WRITE CIRCUITS.

Low-going DO WRITE pulses are produced as a result of Plot Absolute (PA) or Text (TX) "program" instructions. DO WRITE tells the Control Board to write X and Y (or text) values to 1351A memory. The Control Board responds with a low-going WRITING signal and a negative-going CHANGE DATA clock.

When A0 (1351A memory address line zero) is low, the Control Board writes X value to 1351A memory following DO WRITE. If Text mode, U50B causes X value to be output as 1023 (ID1-ID10 are high, schematic 2C). This is the Text flag to 1351A Character Generator.

Generation of DO WRITE will be covered by two cases: (1) Plot Absolute; and (2) Text.

CASE 1.

Detection of a Plot Absolute by U27D allows U57C to produce a low-going DO WRITE signal when a ";" (semicolon) is received from RS-232. Prior to the ";" the 1351A should receive X and Y values separated by a "," (comma).

Data byte acquisition from RS-232 is controlled by the Ready For Data Byte sequence for each parameter byte.

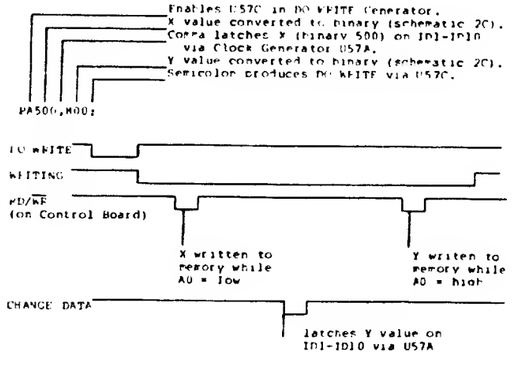


Figure 8-8. Plot Absolute DO WRITE, WRITING, CHANGE DATA Sequence

CASE 2.

Detection of a Text command allows Ready For Text Byte Latch U29B and U22C in the DO WRITE Generator to produce a low-going DO WRITE pulse for each text byte received.

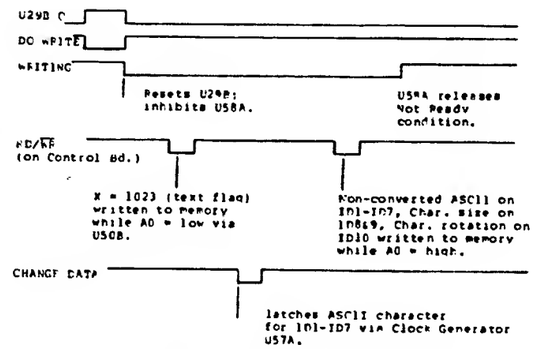


Figure 8-9. Text Mode DO WRITE, WRITING, CHANGE DATA Sequence

8-27. RETURN TO LISTEN FOR PROGRAM.

If 1351A is in Text mode, an ETX (End of Text) is required in order to exit Text mode.

To terminate any instruction (including a previously exited Text instruction) the 1351A requires a ":" (or CR or LF) character from RS-232. This causes U19B output to go low. Listen For Program/Data Latch U1A is reset to "program." Instruction (program) Latches U28 and U21 on schematic 2A are reset.

8-28. PEN ENABLE (Z-AXIS) CIRCUIT.

Pen Enable (PE) "program" instruction is decoded by U20 on schematic 2A. The parameter is converted to binary and is latched on schematic 2C by a "," (comma) from RS-232 via Clock Generator U57A. This becomes the Pen Enable Data Bit which is applied to U27B. This Data Bit is clocked into Pen Enable Latch U35A when U19B output goes low to signal "return to listen for program."

Pen Enable Latch U35A output defines Z-axis status for all 1351A vectors and characters. High = beam on; low = beam off. Z-axis status is sent via the Control Board to the Display Board. From the Display Board, Z-axis status is sent back to the Control Board as PBO1 when A0 = high. This enables/disables 1351A Z-axis output (unless overridden by file blank/unblank bit PBO2).

P/O A2

P/O A3 INPUT/OUTPUT ASSY RS-232 (52105-665011)

PEN ENABLE LATCH

2A 22 H=E FROM U2D (11)

2C 27 H=PEN ENABLE DATA BIT

2A 21 L=E

2A 20 L=P

18 H=P

17 2A 2A

U27B U27C U26B U36D U26A U35A FF NC NC

L=CR OR LF OR

INSTRUCTION LATCH CLOCK GENERATOR

U37F C46 .51 R54 2700 R55 2200 +5V U30B

H=LISTEN FOR DATA(TEXT OR PARAMETER)

H=LISTEN FOR PROGRAM

R14 47K Q2 R15 180 R17 180 Q1 R16 47K E B C

LISTEN FOR PROGRAM DATA LATCH

U90 U1A FF +5V

12 U32(15)

6 U24(8)

26 U9(3) L=RESET

5 U32(7)

4 U16(8)

U37 U238 FF +5V NC NC

U18 FF U220 U79B U79A

POSITIVE =2ND PROGRAM BYTE

READY FOR PROGRAM BYTE LATCH

U17A FF U90 NC

L=RETURN TO LISTEN FOR PROGR

2A

2D 19 U20(6) L=TEXT

58 U76(9) L=ETX

8 U64(8) L=ETX

U30A +5V L=ETX

U37 H=CR OR LF OR

U19B U29A FF NC

TEXT MODE LATCH

READY FOR TEXT BYTE LATCH

U50C U50B U29B FF

P/O XA3P1 P/O P1

3 42 FROM CONTROL BD

L=WRITING

2A 25 TOU23(3)

3 43 42 L=CTRL BUSY

14 L=;(SEMICOLON)

4 44 46 FROM DISPLAY BD

A0(L=X/H=Y)

U36C U50D R8 2700 C4 51 R9 2200 +5V

C9 200

U37

DATA ENABLE AFTER PROGRAM CONTROLLER

U8B

U8B FF U15C +5V R10 2700 C5 51 R11 2200

L=ETX

U22C U38D U35B FF NC

U57C R12 2700 C6 51 R13 2200 +5V

DO WRITE GENERATOR

U30C

2D

2A 28 CLK 2

L=P

2A 24 U20(9) L=A

15 U14(11) L=,(COMMA)

3 45 44 FROM CONTROL BD

L=CHANGE DATA

U27D 12 13 11 L=PA

DATA/TEXT SELECTOR& LATCH CLOCK GENERATOR

U27A U57B U57A

P/O A2

L=ETX OR IFC (L=CLEAR INSTRUCTION LATCH) → 10 2A TO U79(9)

Z-AXIS (H=PE1/L=PE0) → P/O P1 33 → P/O XA3P1 → 46 TO CONTROL BD 3

L=DATAL → 53 → 47

L=PROGL → 51 → 48

TO FRONT PANEL LEADS

+5V 14/7 ALL IC SUPPLY CONFIGURATIONS

LOGIC DEVICE POWER CONNECTIONS

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC "1"=H
   0V TO +0.8V=LOGIC "0"=L

INSTRUCTION LATCH CLOCK GENERATOR

U37F, U30B, R54 2700, C46 .51, R55 2200, +5V

EN FOR DATA (TEXT OR PARAMETER)

R14 47K, Q2, R15 180, R17 180, Q1, R16 47K, E B C

H=LISTEN FOR PROGRAM

TO U22(2) → 29 2C

P=2ND PROGRAM BYTE CLK TO U21(9) U19(10) → 11 2A

P=1ST PROGRAM BYTE CLK TO U28(9) → 13 2A

U18, U22D, U79B, U79A

POSITIVE =2ND PROGRAM BYTE

READY FOR PROGRAM BYTE LATCH

U17A, U9D, NC

L=RESET

NOT READY CONTOLLER

U58A, R18 2700, R19 2200, C7 51, U16B, P=RNCR → 2 2A

L=RETURN TO LISTEN FOR PROGRAM → 9 2C

READY FOR TEXT BYTE LATCH

U50C, U29B, U50B

L=TEXT MODE → 30 2C

H=TEXT MODE

H=TEXT=L=BINARY DATA → 7 2A

→ 31 2C

H=OUTPUT X AS 1023 (TEXT FLAG) → 32 2C

L=DO WRITE → 33 2D

→ 48 → 49 3 TO CONTROL BD

L=ETX

U22C, U38D, U35B, NC

U57C, +5V, R12 2700, C6 51, R13 2200

DO WRITE GENERATOR

U8B, R10 2700, C5 51, R11 2200, U15C, +5V

U30C

U8A

READY FOR DATA BYTE LATCH

U8A

U33A, U33B, NC

+5V, R20 2700, C8 51, R21 2200

FOUR STATE COUNTER

U33

→ 34 2C

→ 35 2C

BLE
RAM
LER

L=PA

U27A

DATA/TEXT SELECTOR& LATCH CLOCK GENERATOR

U57B, U57A, U1B

NEG=LATCH OUTPUT DATA → 36 2C

TO U37(1),62(11) U56(11),22(4)

PARTS ON THIS SCHEMATIC

P/O A3

C4-9,46
Q1-2
R8-21,54,55
U1,8,90,10F,15C,16B,17A,19B,22C0
U23B,26,27,29,30ABC,33,35
U36C0,37BC0F,38D,50BC0,57ABC,58A,79AB

1351A/132/RS23/8/26/81

2B

Figure 8-10.
Schematic 2B
8-11

8-29. SCHEMATIC 2C PRINCIPLES OF OPERATION.

Schematic 2C contains: (1) Parameter Shift Register/ Text Latch; (2) BCD-to-Binary Converter (for parameters); (3) Parameter or Text Selector and Latch; (4) Character Size and Rotation Latch; and (5) Output Selector circuits.

Operation of circuits on schematic 2C will be covered for two cases: (1) 1351A receiving parameter(s); and (2) 1351A receiving text.

8-30. CASE 1. 1351A RECEIVING PARAMETER(s).

In "listen for data" mode, the four LSBs (DIO1-DIO4) of each parameter byte are converted from Binary Coded Decimal (BCD) to binary. This is because the four LSBs of the ASCII code for digits is in BCD.

This conversion process continues for each digit in the parameter until a "," (comma) is received from RS-232. The "," delimits (bounds) the parameter value by latching the binary result of the conversion for output to the Control Board. If a Plot Absolute (PA) comand was received, then the "," latches the binary value of the X parameter and a CHANGE DATA signal (schematic 2B) from the Control Board latches the binary value of the Y parameter (in response to a ";" from RS-232).

NOTE

Several vectors may be entered following each PA command. For example, "PA100,300; 200,500; 300,800;400,1000;;". This draws four vectors.

BCD TO BINARY CONVERSION.

The Parameter Shift Register Text Latch (U39-U42) is placed in its shift register mode if Text Mode Latch U29A (schematic 2B) does not receive a text command. Data selector U34 converts DIO1-DIO4 from parallel to serial. Each serial DIO value is shifted through U42, U41, U40, and U39 by CLK2.

CLK2 is turned on by Ready For Data Byte Latch U8A (schematic 2B). Four CLK2 pulses are produced for each digit in the parameter. Each digit in the parameter gets shifted down through the cascaded shift register by subsequent CLK2 bursts. For example, if a parameter contains three digits, the first digit will be in U40, the second in U41, and the third in U42.

Parameter Shift Register (U39-U42) outputs are automatically converted to binary by the full-adder network of the BCD-to-Binary Converter (U44-U49, U51-U54).

Binary parameter value (CD1-CD14) is selected at Parameter or Text Selector and Latch (U56, U62, U63) when Ready For Text Byte Latch U29B (schematic 2B) signals that the 1351A is NOT in Text mode.

Latch Converted Parameter For Output.

The binary value of the parameter is latched for output at the Parameter or Text Selector and Latch (U56, U62, U63). The latching clock signal comes from Clock Generator U57A on schematic 2B.

This clock is produced when a "," (comma) is received from RS-232 or when the Control Board produces a CHANGE DATA signal (schematic 2B).

For a Plot Absolute, the comma latches the X binary value and the CHANGE DATA latches the Y binary value.

Character Size And Rotation.

When a Character Size (CS) command is detected by U20 on schematic 2A, the input to U36B pin 5 goes low. This enables U36B. Next, the CS parameter is converted to binary and latched into U56 by a "," (comma) from RS-232. When the 1351A receives a ";" (or CR or LF) the CS command is delimited (completed). U36B clocks the CS parameter into Character Size and Rotation Latch U55 to preserve this preconditioning for any subsequent Text (TX) commands.

8-31. CASE 2. 1351A RECEIVING TEXT.

In Text mode, ASCII DIO bytes (received from RS-232 while 135IA is in "listen for data" mode) are not converted to binary. Each unconverted ASCII byte is latched and presented to the Control Board (along with the character size and rotation bits) immediately following the text flag.

The text flag is generated by setting ID1-ID10 lines all high (= 1023) when memory address line A0 is low. Following the text flag, ID1-ID10 are defined as follows when A0 goes high:

ID1-ID7 = ASCII character
ID8 & ID9 = character size (1,2,4,8)
ID10 = rotation bit (low = 0; high = 90 degrees).

Latch Unconverted Text Byte For Output.

Parameter Shift Register/Text Latch (U39-U42) is placed in its parallel latch mode when Text Mode Latch U29A on schematic 2B receives a Text command.

The 8 DIO bits are latched into U41 and U42 by Ready For Text Byte Latch U29B on schematic 2B.

Unconverted ASCII (DIO1-8) is selected at Parameter or Text Selector and Latch (U56, U62) by Ready For Text Byte Latch U29B on schematic 2B. This is the same signal that clocks U41 and U42.

After being selected, the unconverted ASCII byte is latched into the Parameter or Text Selector and Latch (U56, U62, U63) by a CHANGE DATA signal (schematic 2B). N=Latch Output Data is produced on 2B by U57A.

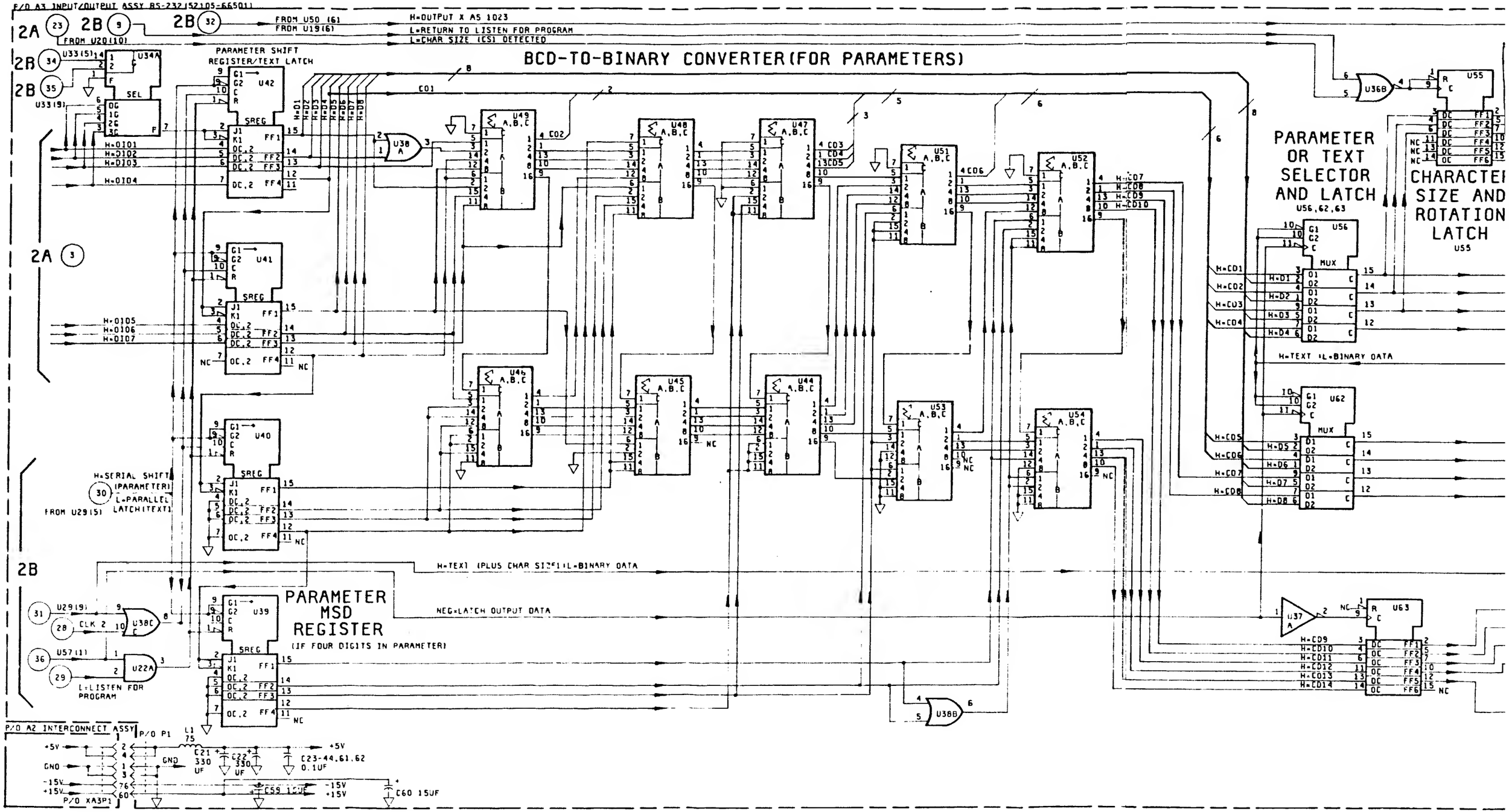
OUTPUT SELECTOR OPERATION IN TEXT MODE.

In Text mode, Ready For Text Byte Latch U29B on schematic 2B causes a DO WRITE signal to be sent to the Control Board. After the DO WRITE, the Control Board writes an X value from ID1-ID10 to 1351A memory when A0 is low.

U50B on schematic 2B causes Output Selector U59-U61 to turn off when A0 is low in Text mode. The Output Selector is turned off by setting its "F" (tri-state) high. Since ID1-ID10 are pulled high via U89 and U90, the X value = 1023. This is the text flag.

Following a CHANGE DATA signal from the Control Board, a Y value is written to memory when A0 goes high. In this case, the Y value is defined as ASCII plus character size and rotation since the X value was the text flag.

U50B turns the Output Selector back on when A0 goes high. The ASCII character bits from U56 and U62, along with character size and rotation bits from U55, are selected for output on ID1-ID10 by Ready For Text Byte Latch U29B on schematic 2B.


P/O A3 INPUT/OUTPUT ASSY 85-232/52105-66501
2A (23) 2B (9) FROM U20(10)
2B (32) FROM U50 (6) FROM U19(6)
H=OUTPUT X AS 1023
L=RETURN TO LISTEN FOR PROGRAM
L=CHAR SIZE (CS) DETECTED
BCD-TO-BINARY CONVERTER(FOR PARAMETERS)
PARAMETER SHIFT REGISTER/TEXT LATCH
2B (34) U33(5)
2B (35) U33(9)
U34A
SEL
H=0101
H=0102
H=0103
H=0104
U42
SREG
H=D1 H=D2 H=D3 H=D4 H=D5 H=D6 H=D7 H=D8
CO1
U38A
U49 A,B,C
U48 A,B,C
U47 A,B,C
U51 A,B,C
U52 A,B,C
U46 A,B,C
U45 A,B,C
U44 A,B,C
U53 A,B,C
U54 A,B,C
4 CO2
4 CO3
1 CO4
13 CO5
4 CO6
H=CO7
H=CO8
H=CO9
H=CO10
NC
U36B
U55
PARAMETER OR TEXT SELECTOR AND LATCH
U56,62,63
CHARACTER SIZE AND ROTATION LATCH
U55
MUX
H=CO1
H=CO2
H=CO3
H=CO4
H=TEXT 1L=BINARY DATA
H=CO5
H=CO6
H=CO7
H=CO8
2A (3)
H=0105
H=0106
H=0107
U41
U40
H=SERIAL SHIFT (PARAMETER) L=PARALLEL LATCH(TEXT)
(30) FROM U29(5)
2B
H=TEXT (PLUS CHAR SIZE)1L=BINARY DATA
NEG=LATCH OUTPUT DATA
PARAMETER MSD REGISTER
(IF FOUR DIGITS IN PARAMETER)
U39
(31) U29(9)
(28) CLK 2
U38C
(36) U57(11)
(29) L=LISTEN FOR PROGRAM
U22A
U38B
U37A
U63
H=CO9
H=CO10
H=CO11
H=CO12
H=CO13
H=CO14
P/O A2 INTERCONNECT ASSY 1
P/O P1
P/O XA3P1
+5V
GND
-15V
+15V
L1 75
C21 330 UF
C22 330 UF
C23-44,61,62 0.1UF
C59 15UF
C60 15UF

RTER(FOR PARAMETERS)

NOTE MANUAL CHANGE
CHAR ROM SELECT

TO U27(5)

H-PE DATA BIT

P/O A2 INTERCONNECT ASSY

(151) 3B

(27) 2B

PARAMETER OR TEXT SELECTOR AND LATCH
U56,62,63

CHARACTER SIZE AND ROTATION LATCH
U55

OUTPUT SELECTOR
U59-61

U89 1800D +5V

U90 1800 +5V

H-TEXT *L*BINARY DATA

H-ROTATE

H-IO1
H-IO2
H-IO3
H-IO4
H-IO5
H-IO6
H-IO7
H-IO8
H-IO9
H-IO10
H-IO11
H-IO12

P/O P1
P/O XA3P1

(50) 3
TO CONTROL BD

P1 PINS NOT CONNECTED

11,13,15,16,26,28,30,32,
34-41,43,47,55,59,61,63-70,
74,75-79,82,84,87-100

NC

LOGIC DEVICE POWER CONNECTIONS

+5V 14 7 U22,36-38

+5V 16 8 U34,39-42,44-49 U51-56,59-63

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC "1"=H
   0V TO +0.8V=LOGIC "0"=L

PARTS ON THIS SCHEMATIC

P/O A3

C23-44,55,60
L1
P/O P1
U22A,34,36B,37A,38A,B,C
U39-42,44-49,51-56,59-63,81

1351A/130/RS232/8/16/81

2C

Figure 8-11. Schematic 2C

8-32. SCHEMATIC 2D PRINCIPLES OF OPERATION.

Schematic 2D contains: (1) CLK1 and CLK2 generators; (2) Power Interrupt detector; (3) TTL Blanking and TTL Blinking circuits; and (4) interface circuits for driving an HP 1338A Tri-color Display (AUXILIARY).

8-33. CLK1 AND CLK2 GENERATORS.

CLK1 runs all the time. U31A divides the 24.6 MHz clock from the Display Board down to 12.3 MHz. The 12.3 MHz CLK1 signal provides the reference for Color Valid Delay Generator U70 and for the Handshake Precision Timing Generator on schematic 2A. CLK1 has to be running for the 1350A to receive bytes from RS-232.

CLK2 runs in four pulse bursts at a rate of 12.3 MHz. U31B produces a CLK2 burst for each parameter byte received from RS-232 via Ready For Data Byte Latch U8A on schematic 2B. CLK2 clocks both the Four State Counter U33 (schematic 2B) and the Parameter Shift Register/Text Latch (schematic 2C) when the 1351A is receiving a parameter byte.

8-34. POWER INTERRUPT DETECTOR.

If a power interruption occurs, the front-panel POWER INTERRUPT LED will be turned on. This indicates a possible deviation from proper 1351A operation. Memory may have been altered or RS-232 instructions may have been misinterpreted.

U68A and Q3 detect interruptions in the +5 V and +12 V power supplies that can occur as a result of line voltage variations. After power-on, U68A Q output is high, turning Q3 on. Q3 collector voltage goes low (Vce approaches 0) to turn on the POWER INTERRUPT LED.

As part of its Initialization program the 1351A should receive an ASCII DC4 character (DC4=20) from RS-232. The DC4 character resets U68A via U14 on schematic 2A. With U68A Q output low, Q3 turns off and the POWER INTERRUPT LED is extinguished.

8-35. TTL BLANKING.

Up to four displays can be driven by the 1351A. These displays can be blanked or unblanked by 16 different combinations of 1351A TTL blanking outputs (DISPLAY 1-4).

The parameter for a Write Auxiliary (WX) instruction determines the TTL blank/unblank combination. The binary value of the WX parameter is inverted on the Display Board and applied to TTL Blanking Latch U67 as PBO3-PBO6 when A0 = high. This blanking information is latched into U67 by the P=Y signal from the Control Board.

Blanking information from U67 is gated with possible blinking signals and latched into TTL Blanking/Blinking Latch U71. U71 is clocked by U77A. U77A introduces an adjustable delay after the Display Board returns VECTOR BUSY signal high. This delay prevents changes in TTL blanking/blinking outputs while the 1351A is drawing a vector.

U71 outputs are inverted by U74 and applied to AUXILIARY and DISPLAY TTL1-TTL4 rear-panel outputs.

Example:

For a "WX0," instruction, the binary value for the parameter is 0000. This is inverted so that PBO3-PBO6 value is 1111. U71 output of 1111 is inverted by U74 so that TTL1-4 output is 0000 (base 2). If four displays are connected, then they will all be unblanked.

8-36. TTL BLINKING.

For WX parameters 8 to 15, Display 4 will always be blanked and Displays 1-3 may be blinked according to settings of Blinking Switch S2. Displays 1-3 are only able to be blinked when unblanked by WX 8-15 combination.

Selected displays (1-3) are blinked at approximately a 4 Hz rate by Blinking Oscillator U78B/U78A. The Blinking Oscillator is started shortly after power-on by a positive edge from U77B. The high level following this positive edge keeps U78A enabled.

U72C output goes low at the 4 Hz rate when enabled by U72D. This 4 Hz signal is gated with selected blanking information to blink displays 1-3 by setting the appropriate TTL outputs high.

8-37. AUXILIARY.

The AUXILIARY connector provides an interface whereby the 1351A can control the color output by an HP 1338A Tri-color Display.

The 1351A must first place the 1338A under Remote control via Auxiliary Remote Enable Latch U76.

Color bits C1 and C2 will now determine the color output of the 1338A. Color codes output by C1 and C2 binary combinations are determined by 1351A file names.

C1 and C2 are latched into Color Bits Latch U65 as File Name bits PBO5 and PBO6. The latching is done by the P=X signal from the control Board.

P=X is then delayed approximately 250 ns by Color Valid Delay Generator U70. After this delay U75A produces a positive edge that tells the 1338A that the color code on C1 and C2 is valid.

The 1338A is prevented from changing colors while the 1351A is drawing a vector. After the 1351A has completed a vector, the Display Board returns VECTOR BUSY high. This causes U75D output to go high, releasing the 1338A to change color if necessary.

The 1338A outputs a COLOR BUSY signal when its color change circuits are active. COLOR BUSY prevents the 1351A from outputting a new vector (U72A output = low) until the 1338A is ready.

Table 8-6. Binary Color Code

File Name	Color	C1 = LSB (Pin 7)	C2 = MSB (Pin 8)
0-15	Green	1	1
16-31	Yellow	0	1
32-47	Red	1	0
48-63	Yellow	0	0

P/O A2 | P/O A3 INPUT/OUTPUT ASSY RS-232 (52105-6650)

FROM DISPLAY 80 — S1 — P/O XA3P1 45 — P/O P1 — L=VECT. BUSY — R22 10 — U66B
FROM CONTROL 80 — 3 — S2 — 86 — P=X — R23 10 — U66C
S3 — 80 — P=Y — R24 10
4 — S4 — FROM DISPLAY 80 — 73 PB04 — 75 PB03 — 71 PB02 — 72 PB01 — R25 10 — R26 10 — R27 10 — R28 10

COLOR BITS LATCH — U65 A FF — U65 B FF
TTL BLANKING LATCH — U67
L=BLANK TTL 4 AND ENABLE TTL 1-TTL 3 BLINKING
H=VECTOR BUSY
P/O A3 — P/O P1 — 83 — P/O XA3P1 — 141 — 81 — 140 — 4B
P/O A2
F — S3 — X

R38-41 ALL 4700 — R38 — R41 — U69A — U69B — U69C — U69D
P/O S1 BLINKING

U77A — R42 1000 — R43 100K — C16 10 — BLANKING DELAY ADJ
TTL BLANK/BLINK LATCH — U71 — DC FF
U75B — U75C — U75D — U74A — U74B — U74C — U74D
H=C1 (LSB) — H=C2 (MSB) — R46 10 — CR3 — C19 .1UF — C20 22UF — GND
L=VECTOR BUSY — H=TTL2 — H=TTL1 — H=TTL3 — H=TTL4 — H=BLANK
R49 10K

BLINKING OSCILLATOR 4HZ — U72D — U72C — H=OSC START AFTER POWER-ON
U78B — U78A — R33 100K — C13 3.3UF — R34 100K — C14 3.3UF — R35 100 — C15 .01UF

AUXILIARY REMOTE ENABLE LATCH — U76B
CR2 — R44 100K — C17 3.3 UF — U77B — R45 100K — C18 22UF

L=COLOR BUSY — R47 2200 — R48 2200 — U73F — U72A — R50 10 — L=135DA VECTOR OUTPUT INHIBIT
L=AUX GO TO REMOTE — U75A — P=COLOR VALID
58 — 2B — TO U30(2)
59 — 2A — TO C10

FROM POWER SUPPLY +12V — 58 — VR1 9.09V — C11 0.1UF — R29 470 — U73E — U73D
2A — 16 — FROM U14 (10)

L=OC4(20)=TURN POWER INTERRUPT OFF
R30 1000 — CR1 — R31 1000 — C12 .1UF — U73A — U68A — U68B — NC
P36 47K — Q3 — 1854-0071 — L=POWER INTERRUPT — R37 180

U77 AND U78 TRUTH TABLE

INPUTS			OUTPUTS	
RESET	A	B	0	$\overline{0}$
0	X	X	0	1
X	1	X	0	1
X	X	0	0	1
1	0	↑	⊓	⊔
1	↓	1	⊓	⊔
↓	0	1	⊓	⊔

COLOR VALID DELAY GENERATOR (250 NS MIN)

4 — S5 — FROM DISPLAY 80 — P/O XA3P1 50 — P/O P1 — 24.6MHZ — R32 10 — U66A
2B — 33 — FROM U8(5) — L=READY FOR NEXT DATA BYTE
U31 A FF — U31 B FF — CLK 1 — CLK 2
U70 — U73C
TO U32(9)U25(9) — 1 — 2A
TO U38(10) — 28 — 2C
TO U33(13) — 28 — 2B

12.3MHZ CLK 1
CLK 2 12.3MHZ BURST
12.3MHZ CLK 1
CLK 2

232(52105-665D1)

COLOR BITS LATCH

TTL BLANKING LATCH

TTL BLANK/ BLINK LATCH

BLINKING OSCILLATOR 4HZ

AUXILIARY REMOTE ENABLE LATCH

COLOR VALID DELAY GENERATOR

(250 NS MIN)

LOGIC DEVICE POWER CONNECTIONS

+5V — 16 — U67,70,71 U77,78 — 8

+5V — 14 — U31,65,66,68 U69,72-76 — 7

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC "1"=H
   0V TO +0.8V=LOGIC "0"=L
4. J1-6 AND HARDWARE IS PART OF A3 I/O ASSY

BINARY COLOR CODE

FILE NAME	COLOR	C1(LSB) PIN 7	C2(MSB) PIN 8
16-31	YELLOW	0	1
32-47	RED	1	0
48-63	YELLOW	0	0
0-15	GRN	1	1

U77 AND U78 TRUTH TABLE

INPUTS			OUTPUTS	
RESET	A	B	0	$\overline{0}$
0	X	X	0	1
X	1	X	0	1
X	X	0	0	1
1	0	↑	⊓	⊓
1	↑	1	⊓	⊓
↑	0	1	⊓	⊓

PARTS ON THIS SCHEMATIC

P/O A3

C11-20 CR1-3
J2-6
Q3
R22-50
S1(5-8)
P/DP1
U31,65-75,76B-78 VR1

1351A/131/R5232/8/26/81

2D

Figure 8-12. Schematic 2D